Switchmode Converter Topologies — Make Them Work for You!

INTRODUCTION

Recent years have seen a tremendous expansion in the sales volume and variety of applications for switching regulators. Surprisingly, if one looks at the circuit arrangements most frequently used, only a few different types are represented. The parallel, half-bridge and full bridge quasi-squarewave circuits and the single ended flyback and feedforward converters represent about 95% of what is available in the marketplace today. A bit of research quickly reveals that there are many other circuit topologies, both switchmode (modified squarewaves) and resonant, that are available and which may be superior to the popular circuits in particular applications.

This application note is intended to provide the switching power supply designer with a broad view of the switchmode converter topology options available and to demonstrate synthesis techniques that should enable the designer to invent new topologies which may better suit his particular design problem.

Why We Need New Topologies

There are several reasons for considering new or non-standard circuits:

a. Increasingly, switchers are operating at higher switching frequencies to reduce size and weight. It is now completely practical to operate above 200KHz, and while the more popular circuits will work at these frequencies, they are by no means optimum. It has been shown[1] that some not so common topologies have very definite advantages at high frequencies.

b. Power MOSFETs are rapidly becoming a reality for switchmode converters. The distribution between switching and conduction losses in a MOSFET is quite different from those of a bipolar, and the choice of circuit topology can have a profound effect on the total power loss. Many of the standard circuits are less than optimum when used with MOSFET switches.

c. The switching power supply designer is limited by the capabilities of the components available to him. Because of the efforts of component manufacturers, the performance limits change continuously, but progress is slow and the designer will always be faced with component limitations. Because the electrical stresses on the individual components vary widely with the topology, the choice of topology can be used as a tool to get around some of the limitations in components, and the larger the number of circuit variations available to the designer, the greater the likelihood that an acceptable solution will be found.

d. As switchers find a wider range of usage, more and more special applications that require optimization of a variety of different performance parameters appear. To cope with these applications, the designer needs a wide variety of circuits to choose from so that really effective designs can be created.

e. The power supply industry is becoming increasingly competitive. Manufacturers using a poorly optimized "one circuit for all applications" approach are going to be pushed out of the marketplace by more aggressive and versatile competitors.

f. Requirements on the control of EMI are becoming much more restrictive; the choice of topology can be used to minimize EMI.

g. It occasionally happens that an individual or organization will create a circuit variation that gives a real or imagined competitive advantage for a particular application. The normal course is to immediately patent the circuit to deny its use to a competitor. While the competitor cannot use the original circuit, he may very well be able to apply the manipulative techniques shown herein to the circuit to produce a different and perhaps even better circuit. Conversely, the circuit originator could better protect himself by manipulating his circuit and extending the patent to all possible variations.

Where Do Circuit Topologies Come From?

There are many sources of switchmode converter topologies. The first and most obvious place to look is standard industry practice. The next source is the published literature in the field; an extensive bibliography is included at the end of this application note. A third rich source is the patent and patent disclosure files. A search of the patent files can be tedious, but every so often a really useful circuit or circuit variation will be found.

The next step is to employ synthesis techniques to generate circuits that do not presently exist. A variety of synthesis procedures exists, and the discussion of these procedures is the main thrust of this application note.

By far, the most important source for new circuits is the designer's intuition. The synthesis procedures described herein have not evolved to the point that the designer can define the desired circuit performance and then follow a specified synthesis procedure that will lead directly to the desired solution; and while very useful, the present range of synthesis techniques are still rather clumsy tools that the designer must guide, using his intuition to reach the desired goal.

CRITERIA FOR COMPARING CONVERTER TOPOLOGIES

As will be demonstrated shortly, the literature, patent search and synthesis efforts produce a large and bewildering array of circuit topologies. The number of circuits is so large that there is no way to deal with all of them on a one-at-a-time basis. What is needed is some orderly means to compare circuits quickly, to enable the designer to choose the best circuit for his application. There are several possibilities for simplifying the comparison process:

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1. The circuits can be organized into families sharing common characteristics.
2. The figures of merit for different topologies can be compared. The stress on the various circuit components varies widely from one topology to another. For each topology and component, a normalized component stress figure of merit can be developed that relates the individual component stress to the input and output voltages and currents.
3. Figures of merit relating the amount of inductive and capacitive energy storage required for a given power level can be derived. These figures of merit are very useful for weight and volume trade-off studies.
4. The feedback loop and transient characteristics are an important practical consideration for comparing topologies. The presence of a right half-plane zero in the boost family of converters is an example of a potential stabilization problem.
5. The component count can be a very important figure of merit, especially for powers below 100W. In converters operating below 100W, the component stress is not usually high enough that multiple components or especially high performance components are needed and the primary objective is usually low cost. As the power level goes above 100W however, it becomes increasingly desirable to use topologies that reduce component stress levels even if the component count is higher. The point is that the component count is a very useful figure of merit, but it can be misleading as the power level is increased.
6. The response of the circuit to component nonidealities is a useful point of comparison. For example, the switch conduction overlap caused by transistor storage time can be either harmless or catastrophic, depending on the topology.

Converter Topologies Organized Into Families

It appears that all of the known switching regulators can be synthesized from combinations of three circuit elements: The boost regulator, the buck regulator and some form of DC transformer, as shown in Figure 1. Examples to support this contention will be given in following sections. This observation suggests a family delineation that derives from the basic elements from which a particular converter can be assembled. Figure 2 is a converter family tree that begins with the buck and boost converters as the most basic elements. As will be shown shortly, the buck and boost converters are electrical duals of each other. The DC transformer is not treated as a starting element but is used as a circuit element to produce permutations of the basic buck and boost regulators.

The buck derived family shares the common characteristics of discontinuous input current, continuous output current, duty cycle, $D = V_b/V_i$, non-moving poles in the transfer function and an internal bus voltage V_b lower than V_i. The boost derived family shares the common characteristics of continuous input current, discontinuous output current, a right half-plane zero and moving left half-plane poles in the transfer function, and an internal bus voltage higher than the input voltage. The family of converters made up of combinations of buck and boost converters is not so neatly characterized, because of the diversity of its members, but there are localized generalizations that can be made. Wherever possible, the common name for the particular converter is given. Since many of the entries in Figure 2 are not generally known, or do not have specific names, each entry is referred to the figure number in the following sections where the circuit is first developed.

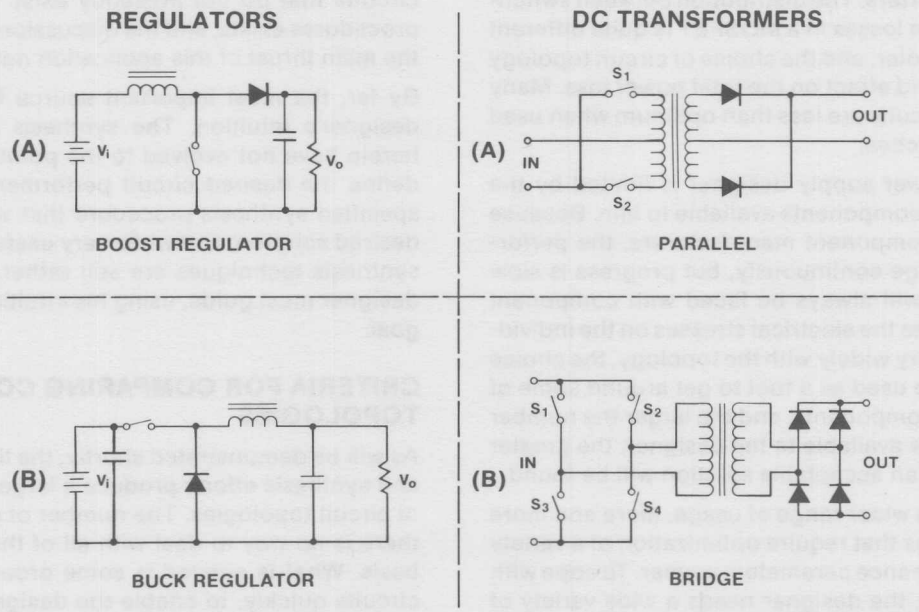


Figure 1

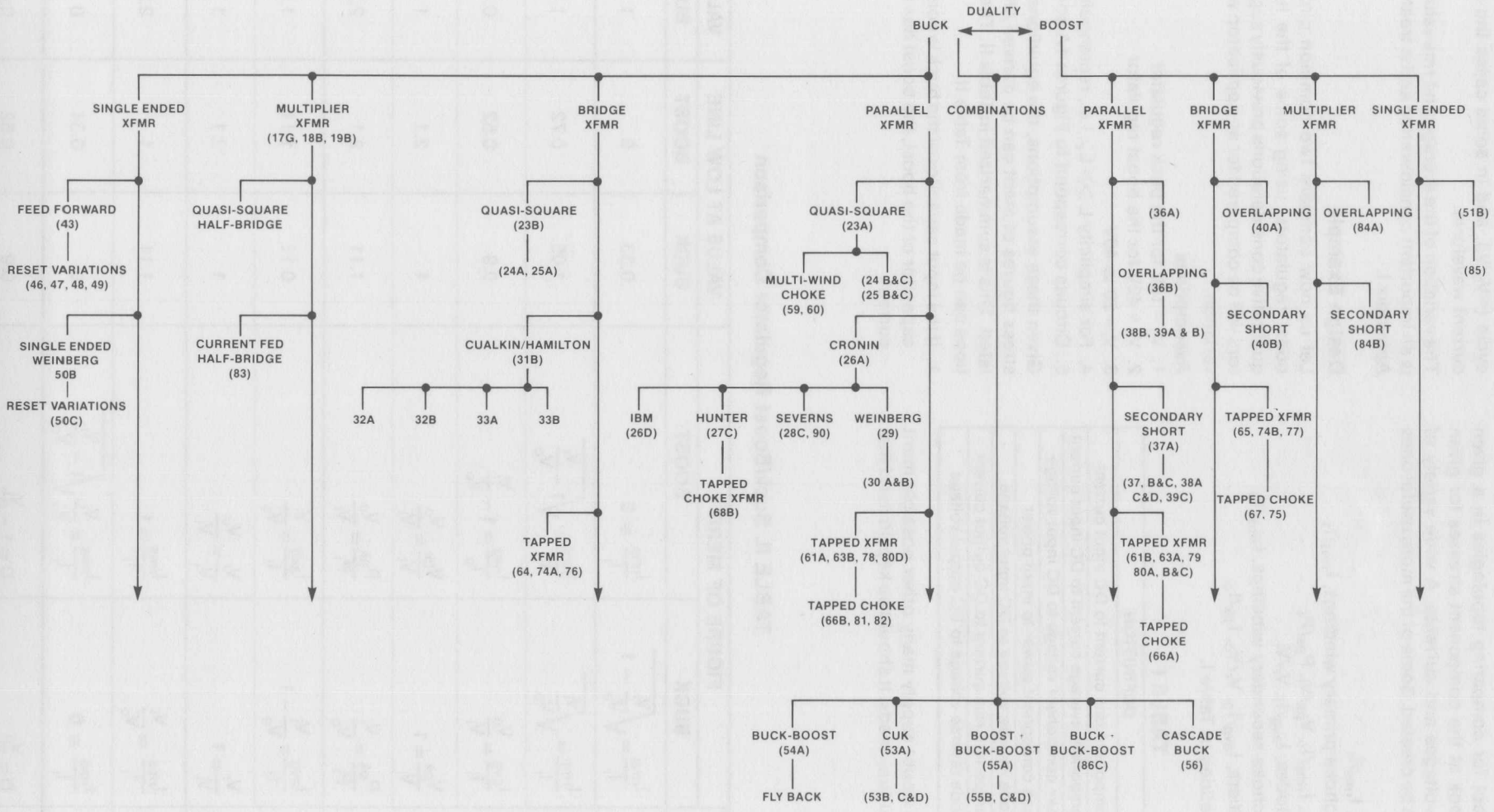

DUALITY
BUCK
BOOST
SINGLE ENDED XFMR
MULTIPLIER XFMR (17G, 18B, 19B)
BRIDGE XFMR
PARALLEL XFMR
COMBINATIONS
PARALLEL XFMR
BRIDGE XFMR
MULTIPLIER XFMR
SINGLE ENDED XFMR
FEED FORWARD (43)
RESET VARIATIONS (46, 47, 48, 49)
SINGLE ENDED WEINBERG 50B
RESET VARIATIONS (50C)
QUASI-SQUARE HALF-BRIDGE
CURRENT FED HALF-BRIDGE (83)
QUASI-SQUARE (23B)
(24A, 25A)
CUALKIN/HAMILTON (31B)
32A
32B
33A
33B
TAPPED XFMR (64, 74A, 76)
QUASI-SQUARE (23A)
MULTI-WIND CHOKE (59, 60)
(24 B&C) (25 B&C)
CRONIN (26A)
IBM (26D)
HUNTER (27C)
SEVERNS (28C, 90)
WEINBERG (29)
TAPPED CHOKE XFMR (68B)
(30 A&B)
TAPPED XFMR (61A, 63B, 78, 80D)
TAPPED CHOKE (66B, 81, 82)
(36A)
OVERLAPPING (36B)
(38B, 39A & B)
SECONDARY SHORT (37A)
(37, B&C, 38A C&D, 39C)
TAPPED XFMR (61B, 63A, 79 80A, B&C)
TAPPED CHOKE (66A)
OVERLAPPING (40A)
SECONDARY SHORT (40B)
TAPPED XFMR (65, 74B, 77)
TAPPED CHOKE (67, 75)
OVERLAPPING (84A)
SECONDARY SHORT (84B)
(51B)
(85)
BUCK-BOOST (54A)
FLY BACK
CUK (53A)
(53B, C&D)
BOOST + BUCK-BOOST (55A)
(55B, C&D)
BUCK - BUCK-BOOST (86C)
CASCADE BUCK (56)

Figure 2

Component Stress Figures of Merit

A very powerful tool for comparing topologies in a given application is to look at the component stresses for given input and output voltages and currents. A wide variety of figures of merit can be created. Some of the more useful ones are:

1. Input capacitor, I_{rms}/I_i
2. Transformer or choke primary windings, I_{rms}/I_i
3. Switches, I_{avg}/I_i, I_{rms}/I_i, V_{pk}/V_i, P_{pk}/P_i
4. Primary catch diodes, I_{avg}/I_i, V_r/V_i
5. Transformer or choke secondary windings, I_{rms}/I_o
6. Secondary rectifiers, I_{avg}/I_o, V_r/V_o, I_{pk}/I_o

The symbols are defined in Table I.

TABLE I

SYMBOL	DEFINITION
I_{rms}/I_i	Ratio of component rms current to DC input current
I_{avg}/I_i	Ratio of component average current to DC input current
V_{pk}/V_i	Ratio of peak component voltage to DC input voltage
P_{pk}/P_i	Ratio of peak component power to input power
V_r/V_i	Ratio of diode reverse voltage to DC input voltage
I_{rms}/I_o	Ratio of component rms current to DC output current
V_r/V_o	Ratio of diode reverse voltage to DC output voltage

The reader can no doubt supply many other possible merit figures to suit individual needs. It should be kept in mind that each of these figures of merit will be a function of the duty cycle ($\propto V_b/V_i$), and in some cases the shape factor of the current waveform.

The variation of the average and rms values of the waveforms is an important consideration and is treated at some length in Appendix I.

Design Example

Let us now compare two common circuits, the buck and boost regulators, using some of the figures of merit and qualitative considerations previously suggested. The regulators will be compared for an applicaton with a two to one line variation.

Assumptions

1. V_o = 18V for the buck regulator
2. V_o = 42V for the boost regulator
3. V_i = 20 to 40V
4. For simplicity $L >> L_c$; i.e., rectangular current pulses
5. Circuits correspond to Figures 1A and 1B

Given these assumptions, the equations for the component stress figures of merit can be derived and the values calculated. This is summarized in Table II. The following observations can be made from Table II.

1. If the input capacitor of the buck is compared to the output capacitor of the boost, the boost has a much lower ripple current.

TABLE II. Buck/Boost Regulator Comparison

COMPONENT	FIGURE OF MERIT		VALUE AT LOW LINE		VALUE AT HIGH LINE	
	BUCK	BOOST	BUCK	BOOST	BUCK	BOOST
C1	$\frac{I_{rms}}{I_i}=\sqrt{\frac{V_i}{V_o}-1}$	$\frac{I_{rms}}{I_i}\cong 0$	0.33	0	1.11	0
S1	$\frac{I_{rms}}{I_i}=\sqrt{\frac{V_i}{V_o}}$	$\frac{I_{rms}}{I_i}=\sqrt{1-\frac{V_i}{V_o}}$	1.05	0.72	1.49	0.22
	$\frac{I_{avg}}{I_i}=\frac{V_o}{V_i}$	$\frac{I_{avg}}{I_p}=1-\frac{V_i}{V_o}$	0.9	0.52	0.45	0.05
	$\frac{V_{pk}}{V_i}=1$	$\frac{V_{pk}}{V_i}=\frac{V_o}{V_i}$	1	2.1	1	1.05
	$\frac{P_{pk}}{P_i}=\frac{V_i}{V_o}$	$\frac{P_{pk}}{P_i}=\frac{V_o}{V_i}$	1.11	2.1	2.22	1.05
D1	$\frac{I_{avg}}{I_i}=\frac{V_i}{V_o}-1$	$\frac{I_{avg}}{I_i}=\frac{V_i}{V_o}$	0.11	1.11	1.22	0.95
	$\frac{V_r}{V_i}=1$	$\frac{V_r}{V_i}=\frac{V_o}{V_i}$	1	2.1	1	1.05
L1	$\frac{I_{rms}}{I_i}=\frac{V_i}{V_o}$	$\frac{I_{rms}}{I_i}=1$	1.11	1	2.22	1
C2	$\frac{I_{rms}}{I_i}\cong 0$	$\frac{I_{rms}}{I_i}=\frac{V_i}{V_o}\sqrt{1-\frac{V_i}{V_o}}$	0	0.34	0	0.21
Duty Cycle	$D=\frac{V_o}{V_i}$	$D=1-\frac{V_i}{V_o}$	0.9	0.52	0.45	0.05

2. The switch rms and average currents are much higher in the buck than in the boost. The peak voltages and powers are nearly equal.
3. The diode average current is significantly lower in the boost.
4. The choke rms current is somewhat higher in the buck.
5. The duty cycle excursion is much larger in the boost.

These comparisons can be shown to be valid between complementary members of the buck and boost families. Surveying these comparisons, one would find the boost converter family to be generally more efficient and have lower component stresses than the buck family.

If, however, one now looks at considerations other than component stress, the boost family is not quite so attractive. The feedback loop transfer function contains a zero in the right half-plane, and the poles in the left half-plane vary with the duty cycle. This makes the boost regulator much more difficult to stabilize, and, if simple control loops are used, can mean degraded transient response. The duty cycle variation in the boost regulator is much larger, and this can be a problem if wide load current and line voltage excursions are specified. In the boost regulator, there will be a current surge when the line voltage is applied, and the output voltage in the beginning is controlled by the source impedance rather than the switch. All members of the boost family display similar behavior even when transformer coupled. The difference for the transformer coupled variations is that the surge current occurs at the onset of the switching action rather than at the application of line power.

SYNTHESIS USING DUALITY

Dr. Slobodan Ćuk[2] has demonstrated the application of the duality principle to switchmode converter topologies. At first glance this work may appear to be an interesting but purely academic exercise. This is not the case. Not only does duality give insight into relationships between topologies, but it is also a very practical tool for synthesizing new circuits.

Review of Dual Graphs and Networks*

"The following is a concise summary of the properties of dual graphs and networks, which is sufficient for understanding the subsequent derivations in the following sections. More detailed expositions of duality theory as applied to graphs and electric networks can be found in many standard textbooks.[3,4]

"Duality theory is generally limited to the special class of graphs called *planar* graphs. A graph G_p is said to be a planar graph if it can be drawn on a plane in such a way that no two branches intersect at a point which is not a node. For example, graph G_p in Figure 3A is a planar graph, whereas graph G_n in Figure 3B is not.

"In a planar graph, *meshes* and *outer meshes* are distinguished. Any closed loop of the planar graph for which there is no branch in its interior is a *mesh.* For example, loops bf, bf, and bf are meshes in the planar graph, G_p, of Figure 3A. Analogously, a loop which contains no branches in its *exterior* is called an *outer mesh,* like loop bf in the planar graph G_p of Figure 3A. In this review the star notation (*) is used to designate the dual graphs, networks and dual components to facilitate easier recognition of duality relationships. However, in the remaining sections it will be left out, since the recognition of dual components will by then be mastered.

*This section is a direct excerpt from the paper[(2)] published by Dr. Ćuk.

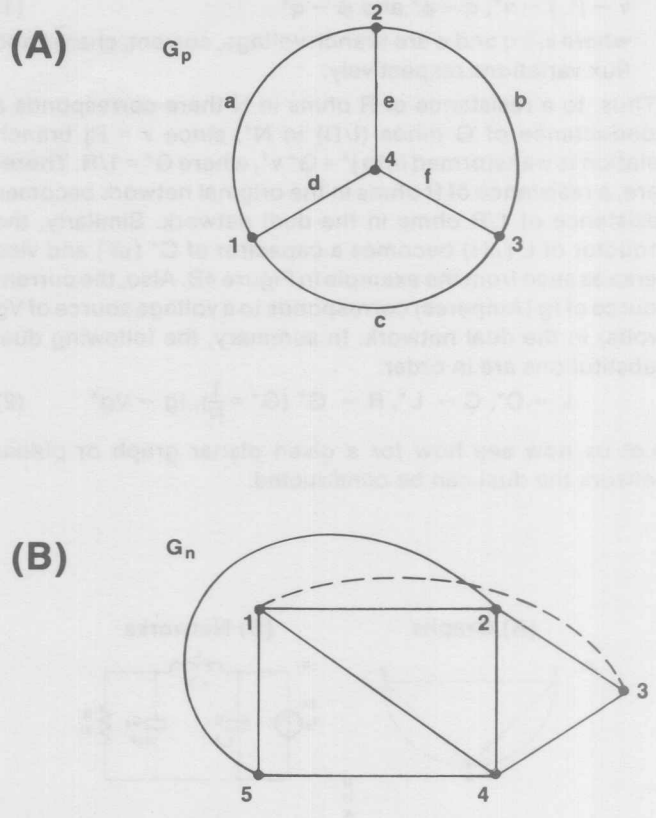


Figure 3: Examples of planar (A) and nonplanar (B) graphs

"Two planar graphs, G and G*, are *dual graphs* if:

a) there is a one-to-one correspondence between the meshes of G (including the outer mesh) and the nodes of G*, and vice versa, and
b) there is a one-to-one correspondence between the branches of each graph, such that whenever two meshes of one graph have a branch in common, the corresponding nodes of the other graph have the corresponding branch connecting these nodes.

"For example, the graphs G and G* of Figure 4A are dual graphs, since the above correspondence can be easily established.

"For two electrical networks, N and N*, to become dual, some additional properties are required. In addition to the graph concepts (meshes corresponding to nodes), the relationships between the dual networks also involve the *dual nature of the elements,* that is, their electrical properties (capacitors corresponding to inductors, voltage sources corresponding to current sources, etc.). Therefore, networks N and N* are dual networks if:

a) they have dual topological graphs G and G*, and

b) the branch equation of a branch of N* is obtained from its corresponding equation of N by performing the following substitutions;

$v \rightarrow j^*$, $j \rightarrow v^*$, $q \rightarrow \phi^*$ and $\phi \rightarrow q^*$ (1)

where v, j, q and ϕ are branch voltage, current, charge and flux variations respectively.

"Thus, to a resistance of R ohms in N there corresponds a conductance of G mhos (I/Ω) in N*, since v = Rj branch relation is transformed into $j^* = G^* v^*$, where $G^* = 1/R$. Therefore, a resistance of R ohms in the original network becomes resistance of 1/R ohms in the dual network. Similarly, the inductor of L (μH) becomes a capacitor of C* (μF) and vice versa as seen from the example in Figure 4B. Also, the current source of Ig (Amperes) corresponds to a voltage source of Vg (volts) in the dual network. In summary, the following dual substitutions are in order:

$$L \rightarrow C^*,\ C \rightarrow L^*,\ R \rightarrow G^*\ (G^* = \frac{1}{R}),\ Ig \rightarrow Vg^* \qquad (2)$$

"Let us now see how for a given planar graph or planar network the dual can be constructed.

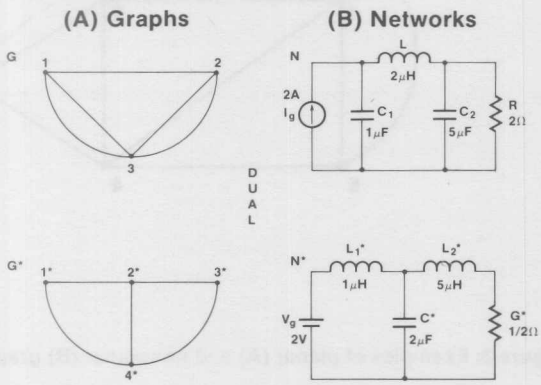


Figure 4: Example of Dual Networks (B) and Their Corresponding Graphs (A)

Algorithm for Dual Graph and Dual Network Construction

The dual graph G* of a planar graph G can be obtained if:

a) to each mesh of graph G, we associate a corresponding node of G*, by placing it inside the mesh. Finally, an additional node is placed outside of graph G (in its exterior) which corresponds to the outer mesh of graph G;

b) for each branch, say b, of G which is common to mesh i and j, we associate a branch b* of G* which is connecting the nodes of G* corresponding to meshes i and j of G.

"This construction is transparent from Figure 5A which is also an example of *oriented graphs*. Given the orientations of the original graph G branches, the orientation of corresponding dual branches is obtained by *counterclockwise* rotation of the original branches until they coincide with their dual branch directions, as also illustrated in Figure 5A.

"The dual oriented network construction involves . . . the (one) additional step of dual substitutions (1) and (2) in the corresponding dual branches . . . Figure 5B.

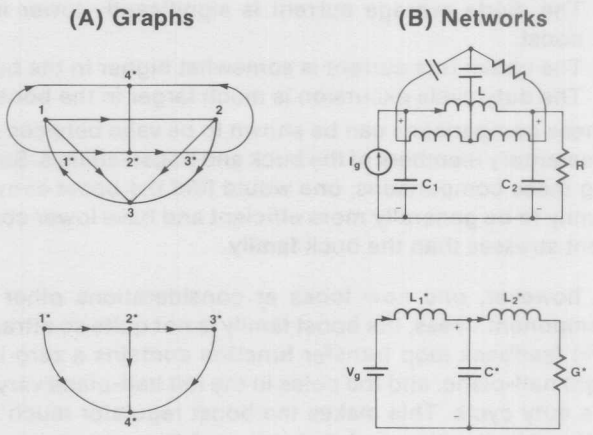


Figure 5: Algorithm for Dual Graph and Dual Network Construction

"The . . . construction of a dual network following this algorithm would have remained just an interesting and elegant topological correlation, had it not been intimately tied with a truly remarkable general law of nature — *the duality principle.*

Duality Principle

"Since many of the results obtained in later sections will be based on (it), the *duality principle,* . . . requires a very careful definition.[3] The remarkable duality principle can be stated as:

> *Consider an arbitrary planar network N and its dual network N*. Let S be any true statement concerning the behaviour of N. Let S* be the statement obtained from S by replacing every graph, theoretic word or phrase (node, mesh, loop, etc.) by its dual and every electrical quantity (voltage, current, impedance, etc.) by its dual. Then S* is a true statement concerning the behaviour of N*.*

"In its abbreviated form, limited to the relationship of its electrical parameters which will be very often used later, it can be stated in the form of the equivalence relationship:

$$S\ (j,v,q,\phi,L,C,Z) \rightleftharpoons (v^*,j^*,v^*,q^*,C^*,L^*,Y^*) \qquad (3)$$

"Duality in Switching DC-to-DC Converters*"

"In order fully (sic) to develop the duality relationships, the notion of a switching DC-to-DC *current* converter needs to be introduced first and its meaning clarified. In other words, a constant *current* input source is postulated in addition to the usual constant voltage source.

Switching DC-to-DC Voltage and Current Converters

"Consider . . . the comparison of the conventional buck converter, with either constant voltage source, as in Figure 6A, or constant current source, as in Figure 6B. In either case, the inductance L is, for simplicity, large enough to result in practically DC current, I, at the output, with negligible switching ripple. Although the practical realization of the switching current converter is of no concern here, it may suffice to say that the constant current source I_g may be voltage limited to prevent excessive rise of the voltage on the input capacitance C (for S at position B only). It is also assumed that ideal

switch S is in position A for interval DT_s and in position B for interval $D'T_s = (1-D)T_s$, where D is the switch duty ratio and T_s the switching period.

"We now concentrate on the principal features of the two converters in Figure 6. For the voltage converter in Figure 6A, we easily obtain in the ideal case:

$$\frac{V}{Vg} = D \tag{4}$$

$$\frac{I}{I_g} = \frac{1}{D} \rightleftharpoons I_g = \left(\frac{D^2}{R}\right)V_g \tag{5}$$

"Thus from (4), the voltage gain is only dependent on duty ratio D, but is *independent* of load R. However, the DC current I_g drawn from the source is dependent on load R as seen in (5). Therefore, the converter of Figure 6A can be conveniently designated as a switching DC-to-DC *voltage* converter. On the other hand, for the converter in Figure 6B:

$$\frac{I}{I_g} = \frac{1}{D} \tag{6}$$

$$\frac{V}{V_g} = D \rightleftharpoons V_g = \left(\frac{R}{D^2}\right) I_g \tag{7}$$

"Here the current gain is independent of load R, as in (6), while both input and output voltage fluctuate to accommodate the change of load R. Thus, this converter can be conveniently designated as a switching DC-to-DC *current* converter. Hence the basic buck power stage operates as either a switching *voltage* or a *current* converter, depending on the type of DC source applied.

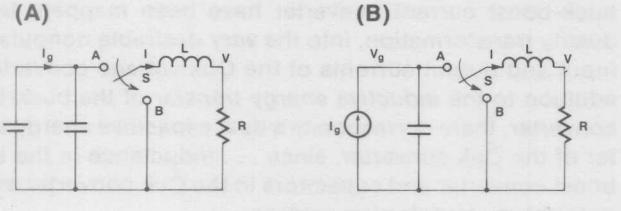


Figure 6: Comparison of a Switching Voltage (A) and a Switching Curent Converter (B)

Duality Among the Four Basic Switching Converter Types*

"Although it has not been demonstrated previously how a dual network of a planar network *which contains switches* can be found, it is relatively simple to resolve this problem. Consider, for example, a switching buck-type current converter more closely, . . . for convenience again redrawn in Figure 7A. For the two positions of switch S (for intervals DT_s and $D'T_s$ respectively), the two switched networks of Figure 7B are obtained. Each of the two switched networks of Figure 7B is a *planar* network, consisting of L, C, R and I_g. Thus, a dual network for each of the two linear switched networks of Figure 7B can easily be found following the algorithmic procedure outlined in the previous section . . . By taking into account the orientation of the branches in Figure 7B, the *dual oriented networks* (of Figure 7C) are obtained. (These two) networks . . . can now be easily redrawn to form a single switching network in Figure 7D for the two positions of its single-pole double-throw switch S.

"An important conclusion can now be made from Figure 7. *The familiar boost voltage converter is just a dual network to the buck current converter.*

"It should be also noted that in the two dual networks, the positions A are the corresponding homologous switch positions. Note also, that for the buck current converter only a minimal configuration was chosen, and the usual output capacitance left out as not essential . . . However, the inductor L **is** essential and leads in the dual network to capacitor C, which is likewise essential for boost voltage converter operation; (see) Figure 7D.

"By (using) the powerful duality principle (3), we can directly obtain the DC voltage gain of the boost converter from the DC current gain (6) of its dual buck converter as:

$$\frac{I}{I_g}\left(\frac{I}{I_g} \rightleftharpoons \frac{V}{V_g}\right) = \frac{V}{V_g} = \frac{1}{D} \tag{8}$$

(assuming) the duty ratio of switch S in Figure 7D is referred to the corresponding position A. However, owing to practical realization of that switch by a bipolar transistor and diode, it is usually referred to position B (on time of the transistor). Thus with the duty ratio defined with respect to B in Figure 7D, we get:

$$\frac{V}{V_g}\Bigg|_{D \rightarrow D'} = \frac{1}{D'} = \frac{1}{1-D} \tag{9}$$

which is the familiar DC gain of the boost converter. This is (the) first example which illustrates the powerful duality principle, and how the property of a dual network (here voltage gain), can be determined directly from the dual property of the original network (here current gain).

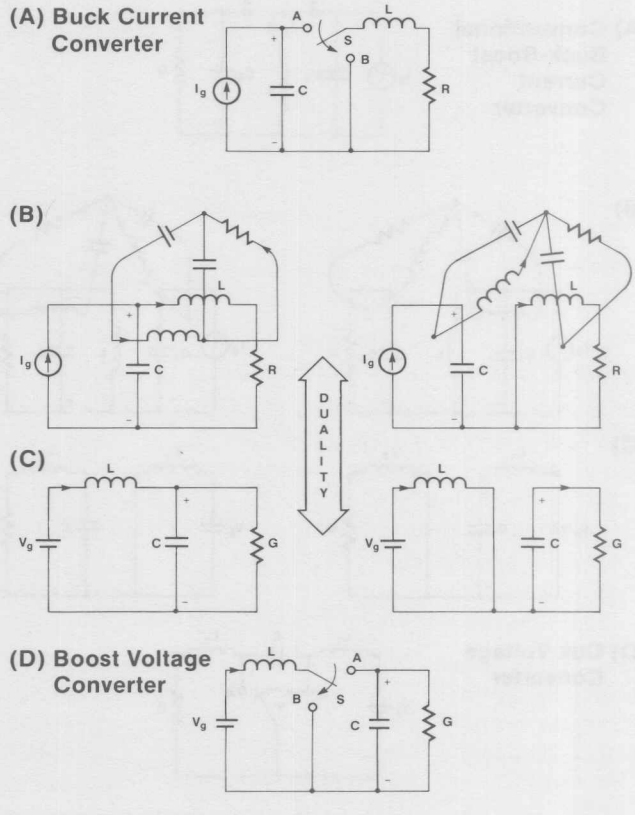


Figure 7: Duality between the Buck and the Boost Switching Converters

"One is now immediately inspired to find dual switching converters to all known switching structures. Once equipped with this powerful tool and method to generate dual switching structures, two goals may be achieved at the same time:

a) the known switching converters can be correlated by a strong bond via duality correlation, and their comparative performance much better understood.

b) new . . . switching configurations may be discovered . . .

"Let us continue this exciting search with the conventional buck-boost converter being the obvious next choice. Again . . . we consider the conventional buck-boost converter as shown in Figure 8A. Following the same algorithm for dual network construction, the dual switched networks of Figure 8C are obtained from the original switched networks of buck-boost converter shown in Figure 8B. Finally, the switching mechanism which leads to the two switched networks of Figure 8C is reconstructed as switch S in the switching converter of Figure 8D. Note that here the use of *oriented* graphs in dual network construction is *absolutely essential,* since only the proper polarity of capacitance C, such as that shown in Figure 8C, leads to the switch S realization , as in Figure 8D. Had the orientation of branches not been used in the duality transformation, the final dual switched networks would leave an ambiguity as to whether the switch implementation is as in Figure 8D.

"The following conclusion can now easily be made from Figure 8. *The dual network of the conventional buck-boost current converter is the new optimum topology (Ćuk) voltage converter.* This now suggests an alternative (deductive) path which could have been followed in the discovery of the new converter topology of Figure 8D . . . The original path of discovery followed quite natural steps of converter performance improvement (cascade of the boost converter followed by the buck converter, hence non-pulsating input and output currents) and simplification with high efficiency in mind (hence reduction of number of switches in a straightforward cascade connection). In any case, both the inductive path and the just-outlined deductive path (coming from the general observation of applicability of the duality principle to switching converters) lead to the same result — the new Ćuk converter topology. Both approaches, however, emphasize the fact that a remaining fourth, very important, member of the family of basic switching converters was missing.

"The establishment of the duality between the two switching converter topologies now permits *all properties* and *results* found for the conventional buck-boost converter to be transferred as dual properties in the Ćuk converter, via the duality principle. Only some of the key essential features and properties will be emphasized here, with the help of Figure 9. For example, the DC current gain of the buck-boost converter $I/I_g = D'/D$ leads to the DC voltage gain of the dual Ćuk converter as:

$$\frac{I}{I_g} \frac{I}{I_g} \rightleftarrows \frac{V}{V_g} = \frac{D'}{D} \qquad (10)$$

when duty ratio D is referred to homologous point A in Figure 8. However, with respect to point B . . . the DC voltage gain becomes:

$$\frac{V}{V_g}\bigg|_{D \longrightarrow D'} = \frac{D'}{D'} \qquad (11)$$

"Comparison of the waveforms in Figure 9 shows that the nonpulsating input and output voltage waveforms of the buck-boost current converter have been mapped, by the duality transformation, into the very desirable nonpulsating input and output currents of the Cuk voltage converter. In addition to the *inductive energy transfer* of the buck-boost converter, there corresponds a dual *capacitive* energy transfer of the Ćuk converter, since . . . inductance in the buck-boost converter and capacitors in the Ćuk converter are the only energy transferring devices.

"In fact, it is this duality of (the) energy transferring mechanism which has prompted the search for the complete duality of (the) switching converter topologies, and subsequently . . . to the establishment of duality as a general concept for a wide class of switching converters.

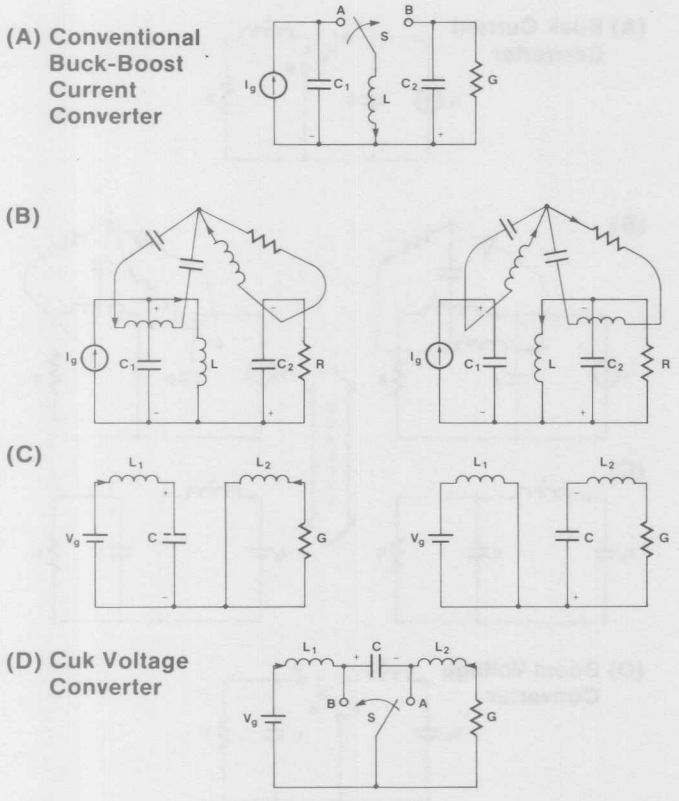


Figure 8: Duality between the Buck-Boost and the Cuk Converters

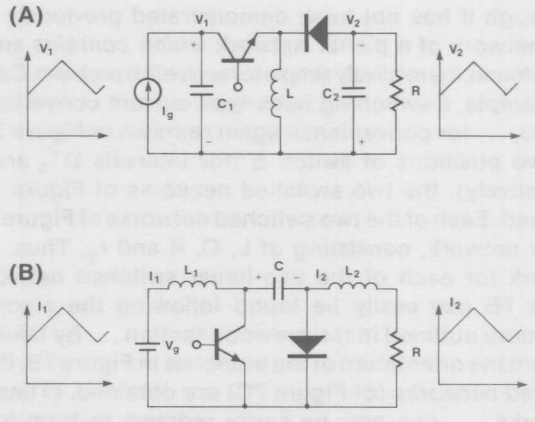


Figure 9: Comparison of Buck-Boost and Cuk Converters

"This also becomes an important distinguishing feature of buck-boost converter types which are based on inductive energy transfer only, and the new Ćuk converters which are primarily based on capacitive energy transfer but . . . not limited to that . . . since some of their extensions (such as coupled-inductor Ćuk converter and single inductor Ćuk converter) possess an additional inductive energy transfer."

Bilateral Inversion**

The duality transformations just discussed can sometimes be difficult to apply in circuits containing transformers, because there is no electrical dual of mutual coupling. Although not as general as the Ćuk method, a simpler duality transformation procedure exists which does not have this problem. It has been demonstrated[5, 6, 7] that the common boost and buck regulators can be made to transfer power from output to input, as well as from input to output (i.e., bilaterally) by the simple expedient of shunting each switch with a diode and each diode with a switch. An example of this is shown in Figure 10, for a boost regulator where Q1 is shunted by D2 and D1 is shunted by Q2. The load is replaced by a source equal to V2; the requirement that V2 > V1 is retained. Switch Q2 is ON when Q1 is OFF. This means that if Q1 operates with a duty cycle of D, then Q2 has a duty cycle of D' = 1-D. The direction of power flow is now a function of D. The procedure can be carried one step further, as shown in Figure 10C; Q1 and D1 are removed from the circuit and source V1 is replaced by a load with a potential of V1 across it.

The circuit in Figure 10C is simply a buck regulator. Again one sees the duality between the buck and boost regulators. The rules for bilateral inversion are as follows:

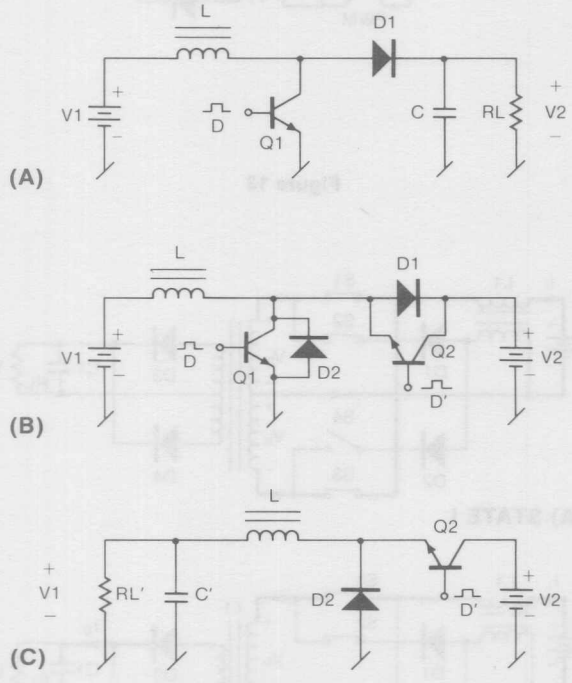


Figure 10

1. All switches are replaced by diodes phased to conduct current in the opposite direction from the original switch.
2. All diodes are replaced with switches phased to conduct current in the opposite direction.
3. If the duty cycle of the original switches is D, then the new switch duty cycle is D' = 1-D.
4. If, for given D, the input voltage is V1 and the output voltage is V2, the original source is replaced by a load with a potential of V1 and the original load is replaced by a source with a potential of V2.
5. For a given D, an original load R_L and output capacitance C, the inverse output load and capacitance is:

$$R'_L = R_L \left(\frac{V1}{V2}\right)^2$$

$$C' = C \left(\frac{V2}{V1}\right)^2$$

6. For particular D, V1, V2 and output power, the value of $L_{critical}$ is unchanged.

The diodes and switches referred to in rules 1 and 2 are only those directly involved in the power conversion process, not those acting as snubbers or other control function.

This inversion process is general, and can be applied to a wide variety of more complex converters. This provides a tool by which new circuits can be derived from known circuits. An example of this procedure for a more complex cicuit is given in Figure 11; the circuit in 11A is a well known voltage-fed configuration (sometimes referred to as a quasi-square wave converter); Figure 11B is the circuit after bilateral inversion is applied. This circuit is a form of a symmetrical transformer coupled boost regulator, in which the switches conduct simultaneously for part of the cycle. A switch timing diagram for circuits A and B is shown in Figure 12.

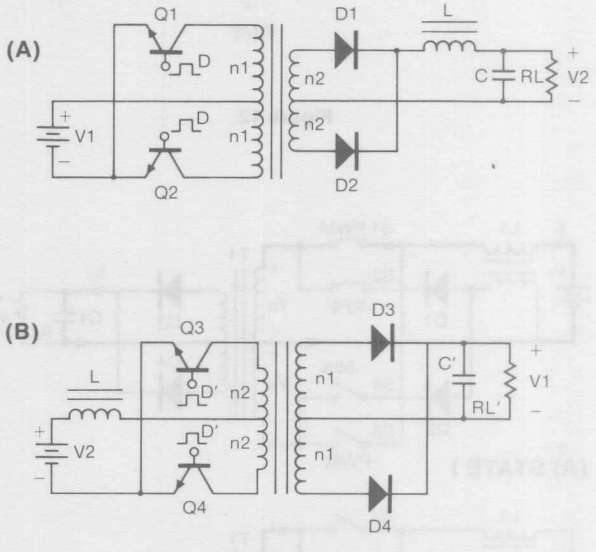


Figure 11

Overlapping Conduction

The use of overlapping switch conduction is not seen very often in present converters, because in many circuits the results are catastrophic. However, in some converters, overlap is not only harmless but can be useful as shown by the example in Figure 12.

**Portions of this section were originally published in the proceedings of the European Power Conversion Conference, 1979.[10]

In many (usually only current-fed) circuits, overlappng and non-overlapping operation may be combined to enhance the circuit's operation. Figures 13, 14 and 15 show an example of such a circuit.

Non-overlapping, Mode A (Figure 14), operation prevails for $V_i \geq V_b$. During STATE I, energy is drawn from the source and then delivered to the load and stored in L. In STATE II, S1 opens and the energy stored in L is delivered to the load. During Mode A, the input current is discontinuous and the load current is continuous.

Overlapping, Mode B (Figure 15), operation prevails for $V_i \leq V_b$. During STATE I, energy is drawn from V_i and stored only in L. During STATE II the energy stored in L is discharged into the load. In this mode the input current is continuous and the output current is discontinuous.

By controlling the switches appropriately, it is possible to design a converter that is a boost regulator at low line voltages and buck regulator at high line.

The foregoing example shows how the basic nature of the converter can be altered, by changing the switch sequence without changing the topology. This technique is not limited to this particular topology but can be used with many other circuits. Figure 16 shows an example where a well known current-fed converter can be made to operate as either a buck, boost or buck-boost converter simply by altering the switch sequence. If a large capacitor is connected from input to output and the switches sequenced for buck-boost operation, the circuit will act as a single inductor Ćuk converter.

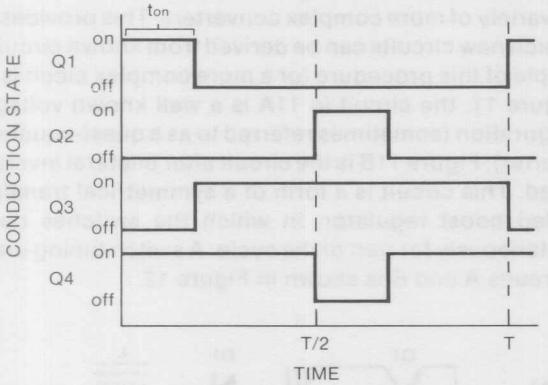


Figure 12

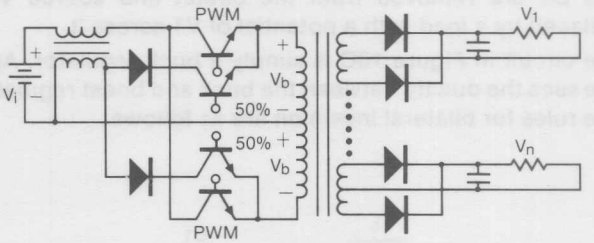


Figure 13

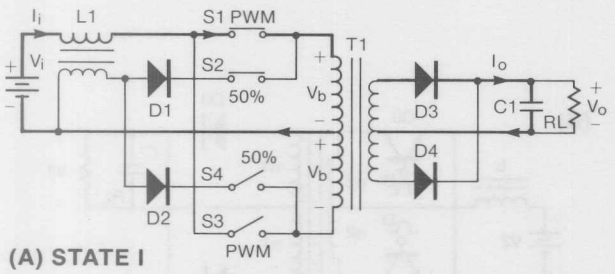


Figure 14

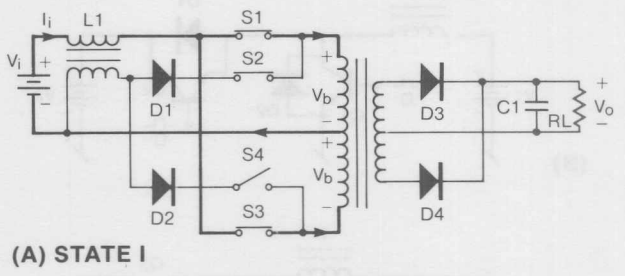


Figure 15

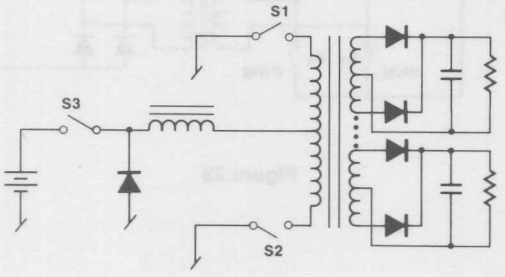
Interchange of Switch Connections

Figure 17 shows four common rectifier connections. It is well known that any one of them can be used on the transformer output, simply by altering the transformer secondary turns and the diode current and voltage ratings. If bilateral inversion is applied to each of the rectifier connections, the result is the switch connections in Figure 17(E-H).

Note that there are a large number of rectifier connections used in practice, but relatively few switch connections. The bilateral inversion principle can be applied to these rectifier connections to generate new switch connections.

The circuit in Figure 17C is a voltage doubler. Another form of doubler is shown in Figure 18A. If this connection is inverted, the switch connection in Figure 18B which results is an alternative to the popular half bridge. This variation is rarely seen in practice but should be useful.

The next step up in this process is to invert a voltage quadrupler, as shown in Figure 19. In the case of the inverted doubler, the switches see the line voltage and twice the line current. For the inverted quadrupler, the switches see one-half the line voltage and four times the line current. This connection would be useful for very high voltage busses. The circuit divides the line voltage across the switches naturally, without the need for complex device matching or voltage sharing networks.



Mode A, Buck Regulator
S_3 = PWM, S_1 and S_2 = 50% conduction

Mode B, Boost Regulator
S_3 = always ON, S_1 and S_2 = overlapping PWM

Model C, Buck-Boost Regulator
STATE I, S_1, S_2, S_3 ON
STATE II, S_2 ON, S_1 and S_3 OFF

Figure 16

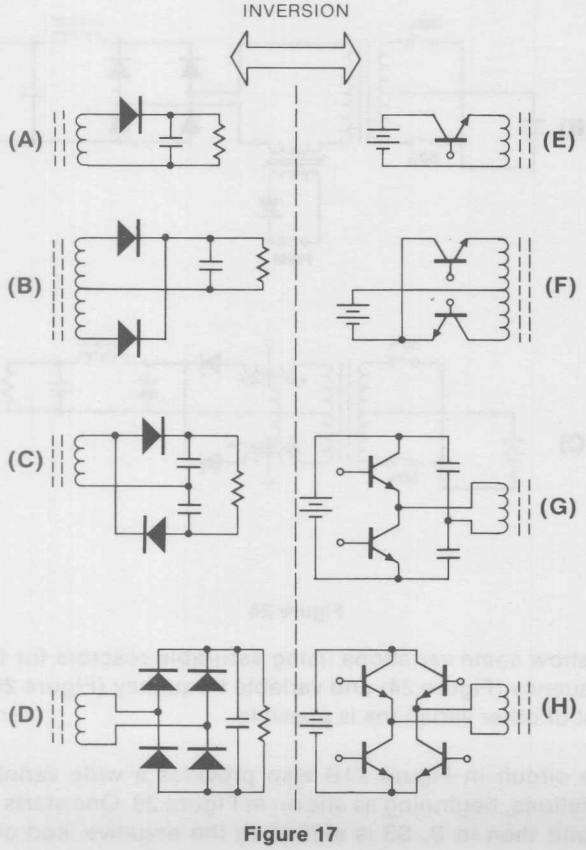


Figure 17

SYNTHESIS USING DC TRANSFORMERS AND BUCK OR BOOST REGULATORS

A wide variety of converter topologies can be synthesized by using a combination of a boost or buck regulator and some form of DC transformer. The DC transformer can take a wide variety of forms, two of which are shown in Figure 20. The function of this circuit element is to provide voltage and current level transformation, either up or down, within the regulator. For the purposes of this discussion, the switches, transformers and diodes are assumed to be ideal.

The Buck Derived Family of Converters

As a starting point let us begin by combining the buck regulator with a parallel connected DC transformer. The buck regulator circuit will be progressively opened at points A through

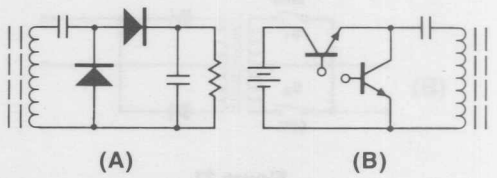


Figure 18

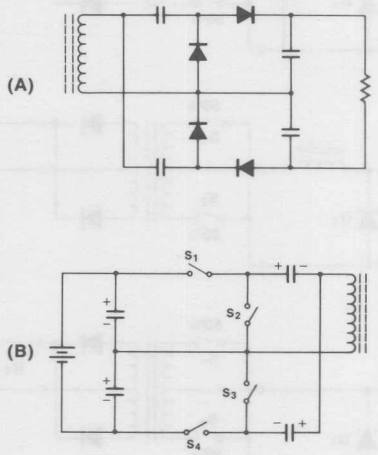


Figure 19

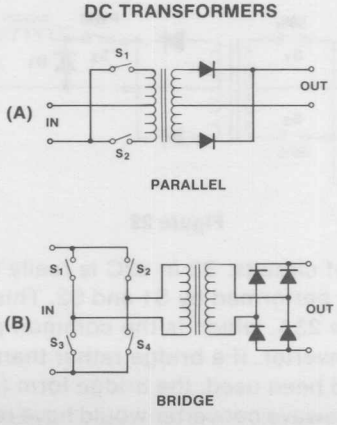


Figure 20

E, and the DC transformer inserted as shown in Figure 21. When this is done, the group of circuits in Figure 22 is generated. Figure 22A is simply a pre-regulator DC-DC converter, 22B is a current-fed DC-DC converter, and 22C and D are essentially identical because the diodes are not needed for the circuit operation. Here is a new circuit apparently, but as will be shown shortly it simplifies into one well known. Figure 22E is a DC-DC converter driving a post-regulator. Circuits 22A and E are dead ends, but 22B and C can be modified to

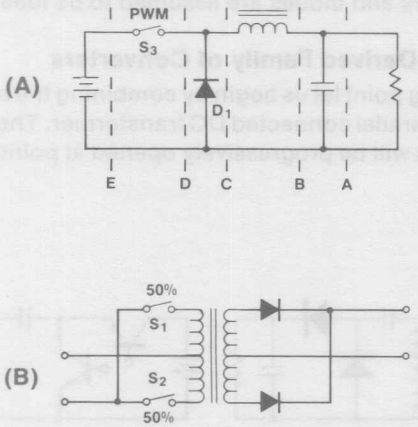


Figure 21

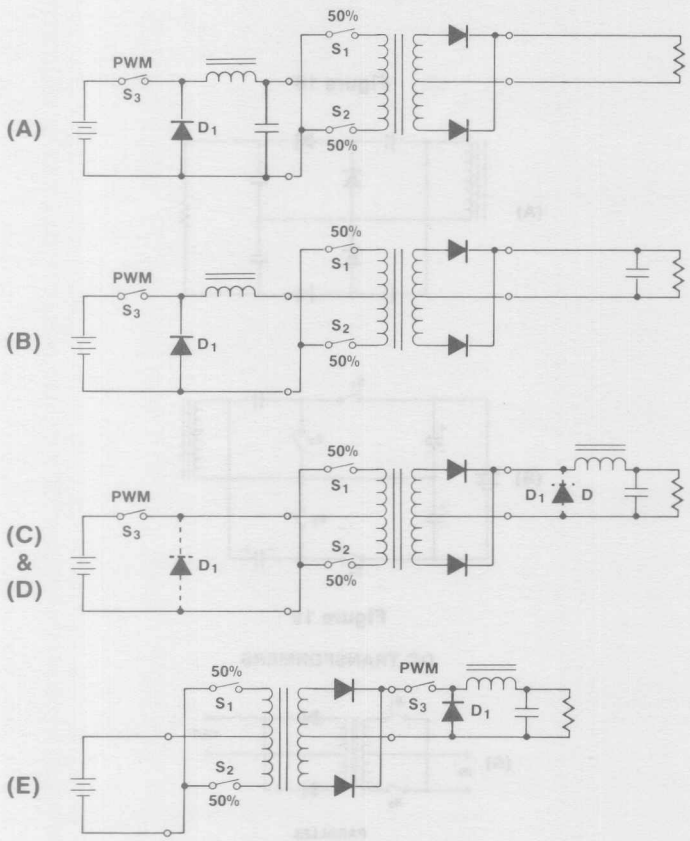


Figure 22

form a variety of circuits. S3 in 22C is really redundant, its function can be performed by S1 and S2. This results in the circuit in Figure 23A, which is the common parallel quasi-squarewave converter. If a bridge rather than a parallel DC transformer had been used, the bridge form (Figure 23B) of the quasi-squarewave converter would have resulted. Figure 23 can be modified in a wide variety of ways; Figures 24 and

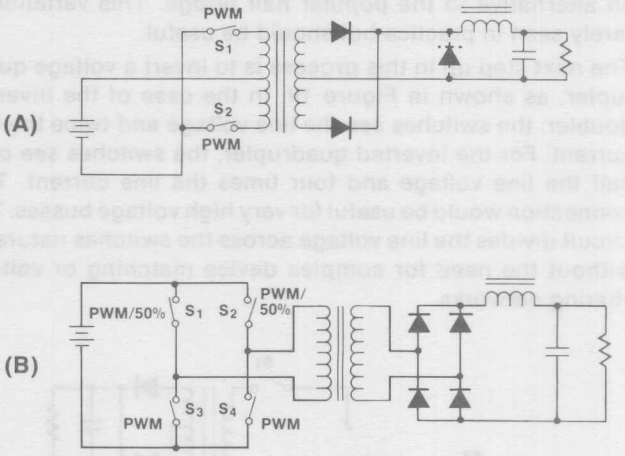


Figure 23

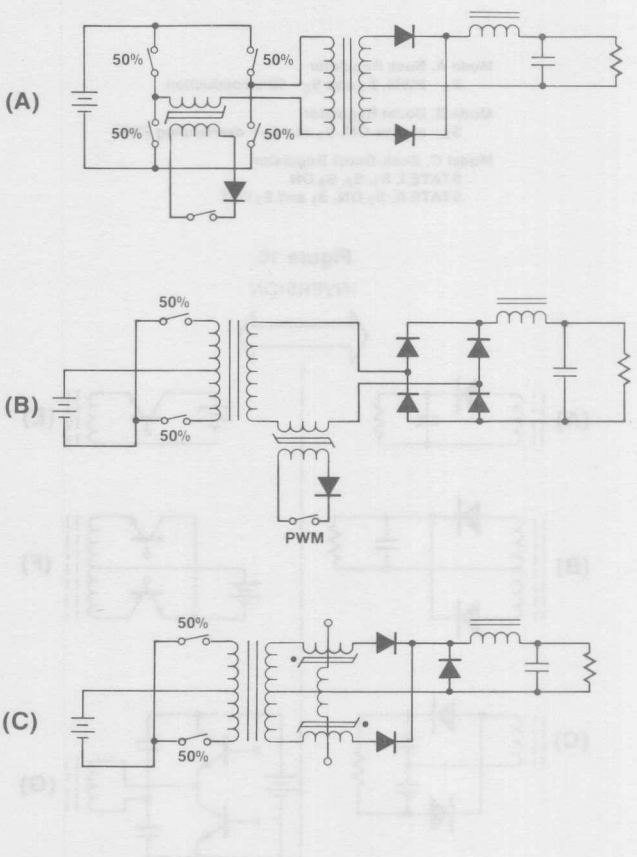


Figure 24

25 show some variations using saturable reactors for fixed frequency (Figure 24) and variable frequency (Figure 25). A host of other variations is possible.

The circuit in Figure 21B also provides a wide variety of variations, beginning as shown in Figure 26. One starts with A, and then in B, S3 is shifted to the negative lead of the

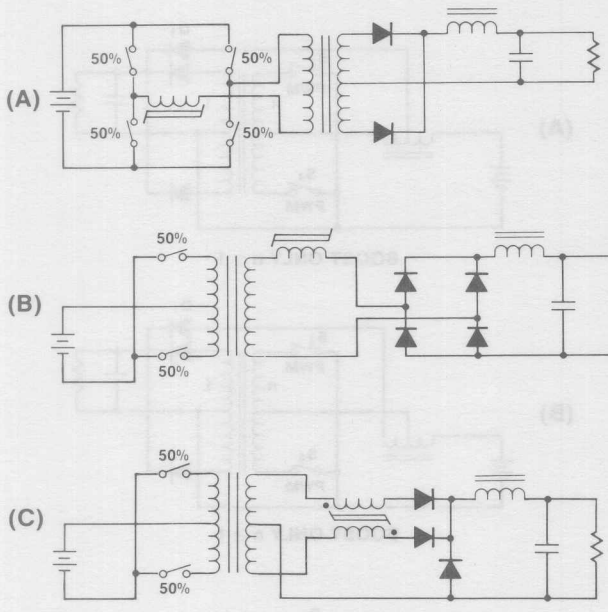


Figure 25

source. In C the connection between S1 and S2 is broken and S4 and D2 added. The result is Figure 26D, which is another current-fed converter. Despite the additional diode and switch, this circuit has some advantages; the PWM switches are referenced to the ground node, the input power is now shared by two transistors instead of one, 100% duty cycle in A corresponds to 50% duty cycle in B. The current in D1, Figure 26A, is commutated by reversing the voltage across the devices. In real devices with finite reverse recovery times, this causes a large current spike to be drawn through S3. In the circuit in Figure 26D, the current in diodes D1 and D2 is commutated by opening their respective series switches, so that when the voltage is reversed across the diode only a very small current spike is present. For high voltage sources the circuit in Figure 26D is very useful, because S3 and S4 see no more than the line voltage and S1 and S2 see only twice the reflected voltage, V_b, which can be made low. For low voltage sources the circuits in Figure 26 are at a disadvantage, however, since there are two switches in series during part of the switching cycle which reduces the efficiency. The circuit can be modified as shown in Figure 27. As before, S1 and S2 conduct alternately, each with 50% duty cycle, and S3 and S4 are modulated. In this circuit the current only flows through one switch at a time, because D1 is reverse biased while S3 is ON; the same applies to D2 and S4 on the other half cycle. The penalty for increased efficiency is that now S3 and S4 will see the line voltage plus twice V_b.

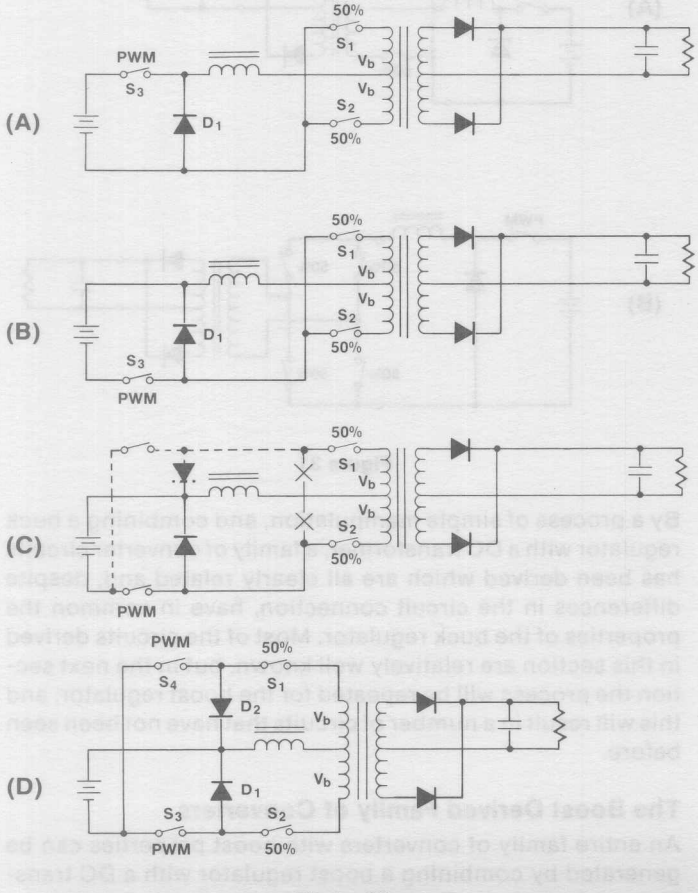


Figure 26

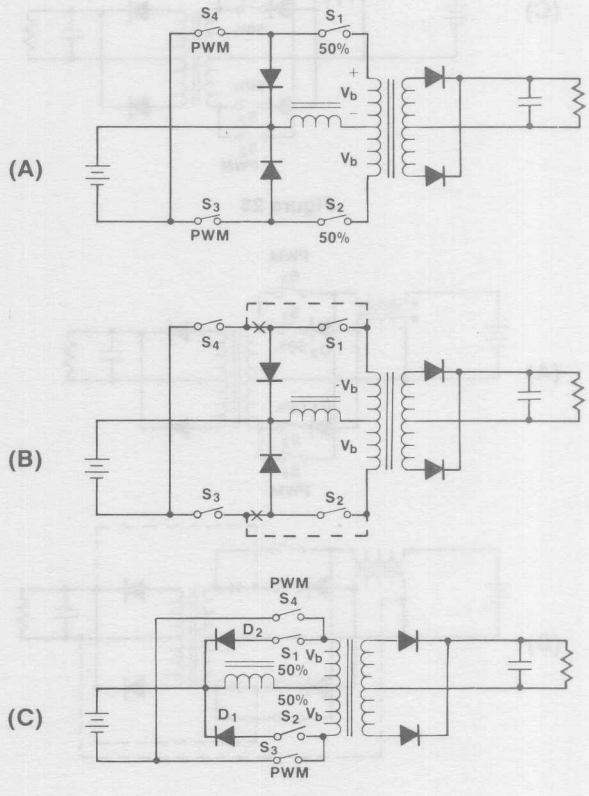


Figure 27

The circuit in Figure 27C can be modified as shown in Figure 28, by using a dual winding choke. This circuit can be further modified, as shown in Figure 29, by connecting one choke winding and the inner switches and diodes to the output. In making this modification, S1, S2 and D2 are no longer necessary; This results in Figure 29C, which is a two switch current-fed converter with the properties of a buck regulator with DC isolation and arbitrary output voltage.

Instead of separate windings on the choke, a tapped winding may be used to produce the variations in Figure 30.

If, in the beginning, a bridge connected DC transformer had been used instead of one which was parallel connected, slightly different circuits would have resulted. For example,

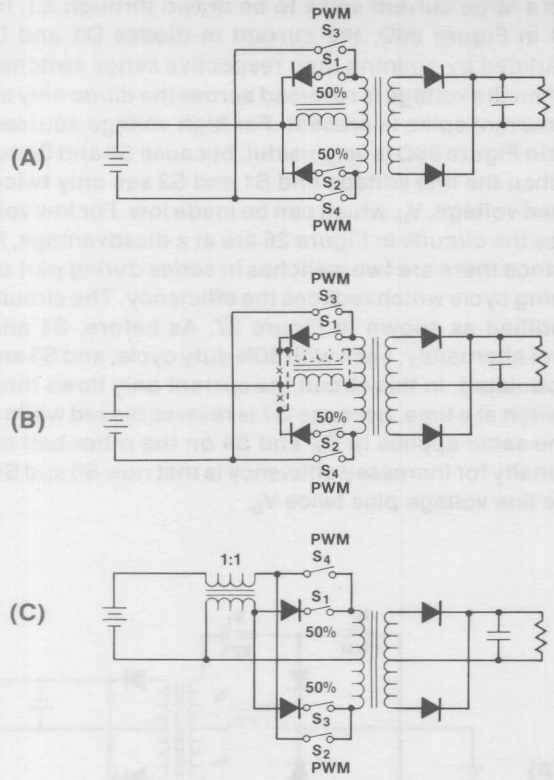


Figure 28

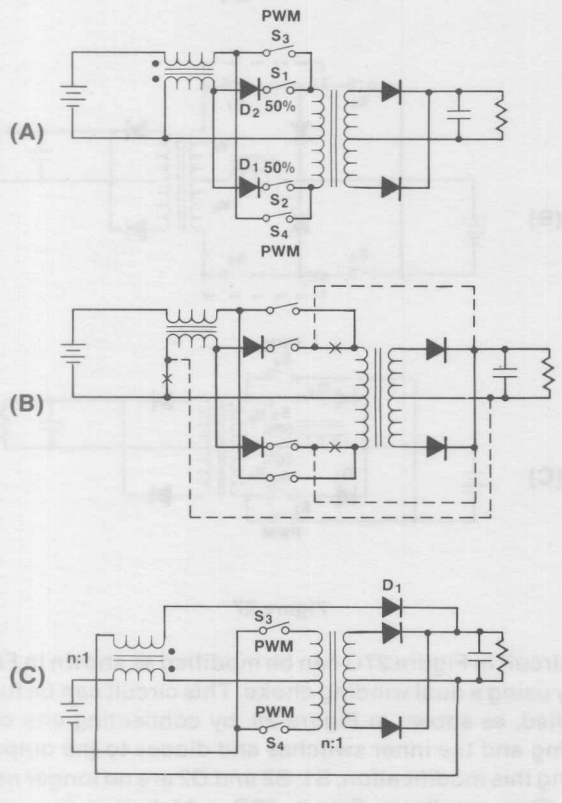


Figure 29

instead of the circuit in Figure 31A, one would have the variation in Figure 31B. This circuit can now be modified, as was done in Figures 26 and 27, to produce the variations in Figure 32. Using a bridge connection, Figure 29 becomes Figure 33A, which is a current-fed bridge inverter. With a bit more manipulation, the circuit in Figure 33B can be derived.

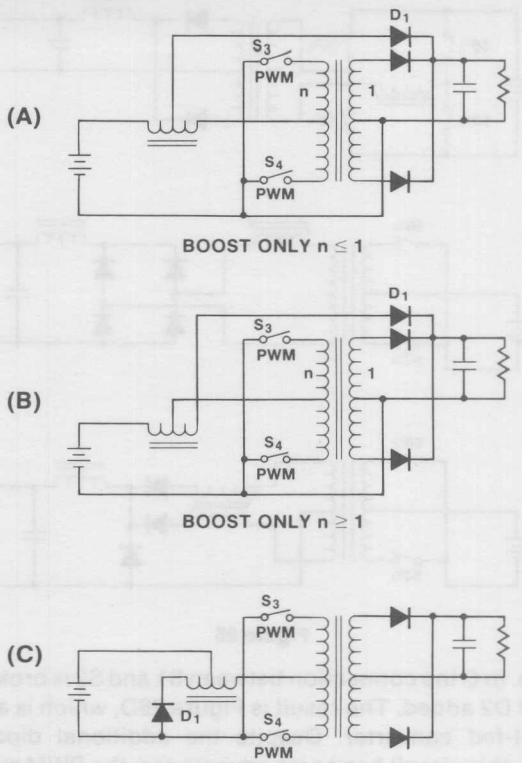


Figure 30

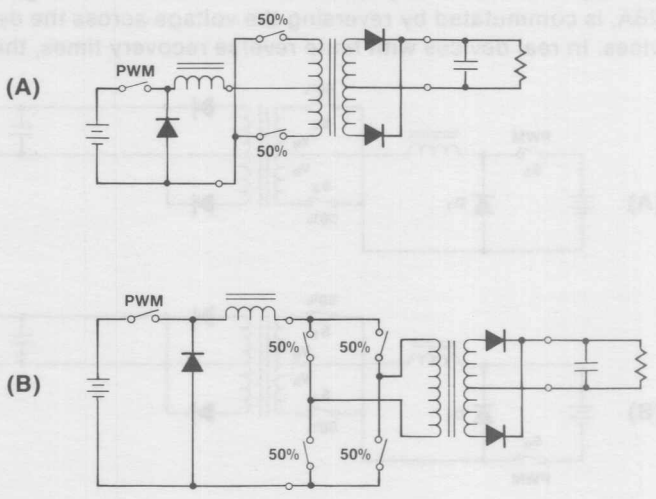


Figure 31

By a process of simple manipulation, and combining a buck regulator with a DC transformer, a family of converter circuits has been derived which are all clearly related and, despite differences in the circuit connection, have in common the properties of the buck regulator. Most of the circuits derived in this section are relatively well known, but in the next section the process will be repeated for the boost regulator; and this will result in a number of circuits that have not been seen before.

The Boost Derived Family of Converters

An entire family of converters with boost properties can be generated by combining a boost regulator with a DC transformer. As before, the DC transformer will be sequentially

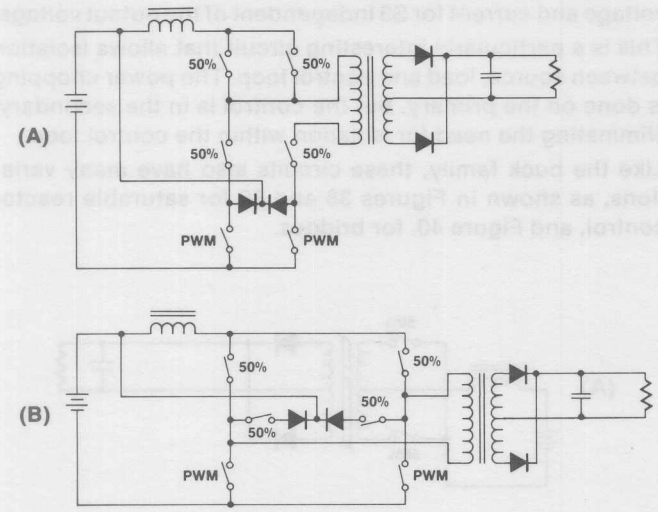


Figure 32

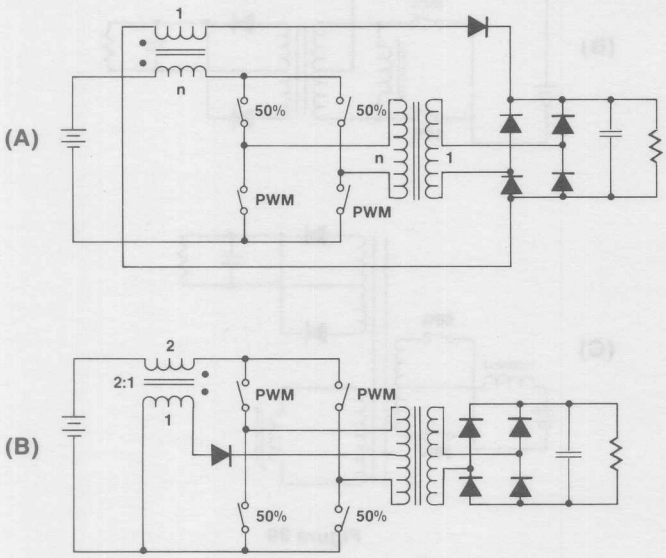


Figure 33

inserted into the regulator (Figure 34). The results of this combination are shown in Figure 35. A is a boost pre-regulator followed by a DC-DC converter. In B and C, the diode D1 serves no function, and can be omitted to form a new circuit. This is a current-fed converter, modulated by periodically shunting the primary. In D, the control element is shifted to the secondary, and the modulation is accomplished by shorting the secondary, again we have a new circuit. The circuit in E is simply a DC-DC converter with a boost post-regulator.

The function of S3 in Figure 36A can be performed by S1 and S2 if S1 and S2 are allowed to have an overlapping conduction interval. This is another way to derive the circuit in Figure 11B.

The circuit in Figure 35D is a usable converter, but it suffers from the disadvantage of having the output current pass through two diodes in series. An alternate and more efficient connection is shown in Figure 37B, where the load current flows through only one diode. The ultimate is reached in Figure 37C, where D1, D2 and S3 are moved to a separate

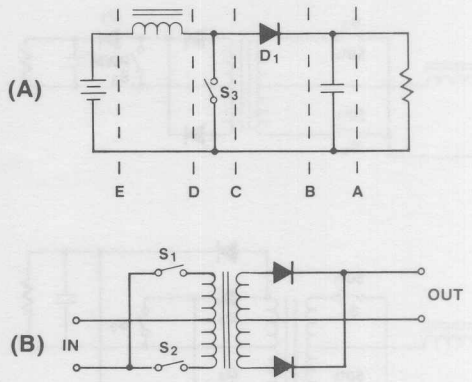


Figure 34

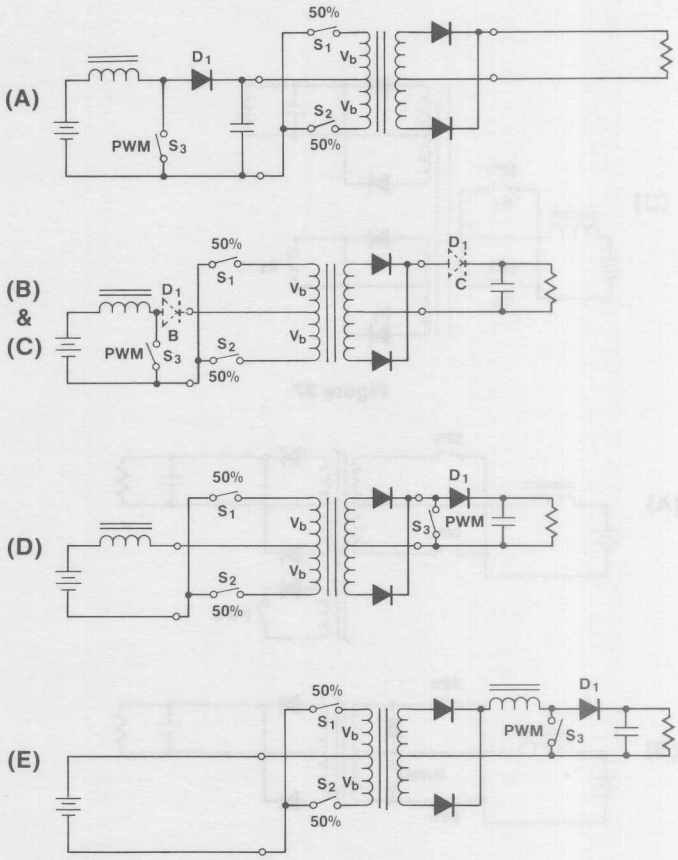


Figure 35

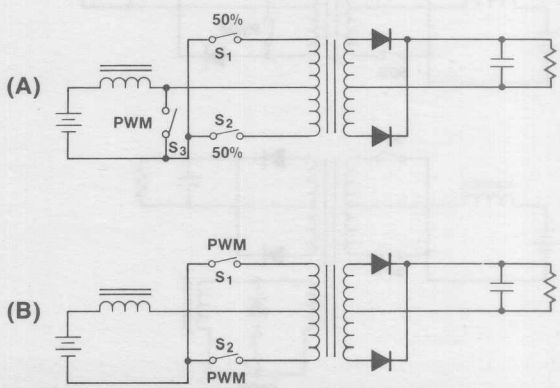


Figure 36

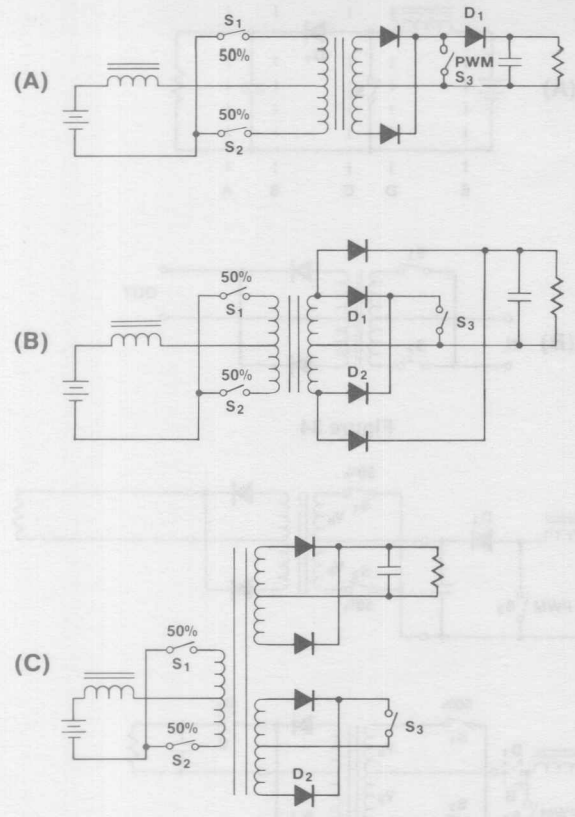


Figure 37

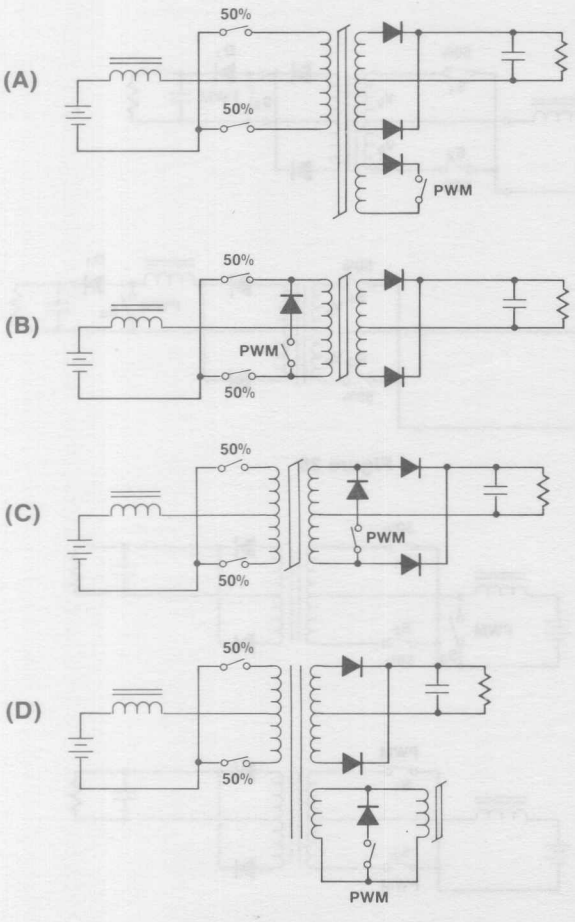


Figure 38

winding, which can be proportioned to provide the optimum voltage and current for S3 independent of the output voltage.

This is a particularly interesting circuit that allows isolation between source, load and control loop. The power chopping is done on the primary, but the control is in the secondary, eliminating the need for isolation within the control loop.

Like the buck family, these circuits also have many variations, as shown in Figures 38 and 39 for saturable reactor control, and Figure 40, for bridges.

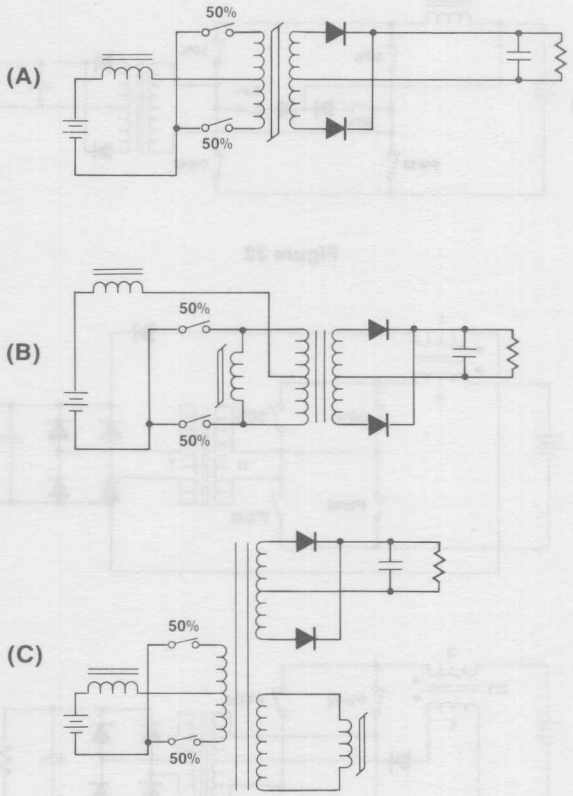


Figure 39

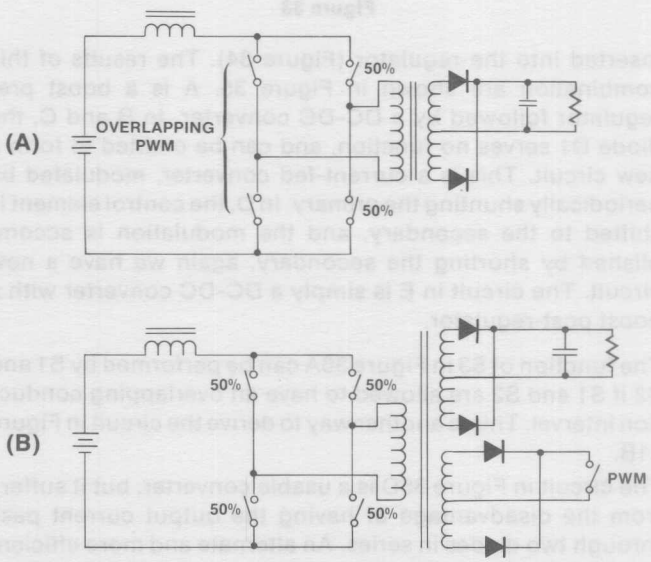


Figure 40

Single Ended Converters

For many applications, low component count is of paramount importance; the family of single ended converters is usually preferred for simplicity. By using a boost or buck regulator combined with a single ended DC transformer, as shown in Figures 41 and 42, if the parallel or bridge DC transformers are divided in half, the result is single ended DC transformers. If these transformers are combined with a buck regulator in manner such as the quasi-squarewave converter, the feed forward converter is the result, as shown in Figure 43. Figure 43B looks a bit strange, and in this form is not really useful, but as will be shown shortly, a minor modification will make it most useful. Both circuits lack one important ingredient, a means for resetting the core. The family of feed forward converters is quite large, but the differences within the family are related to the means by which the core is reset. The basic energy transfer is identical, even though the circuits may look very different.

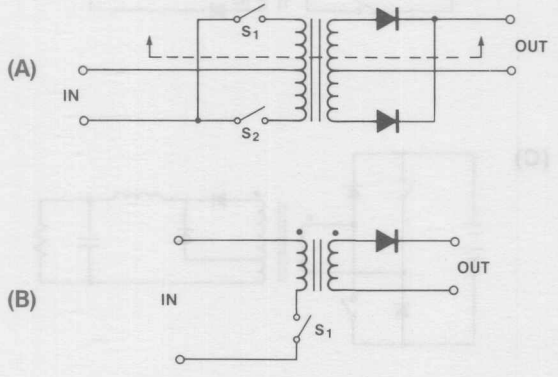


Figure 41

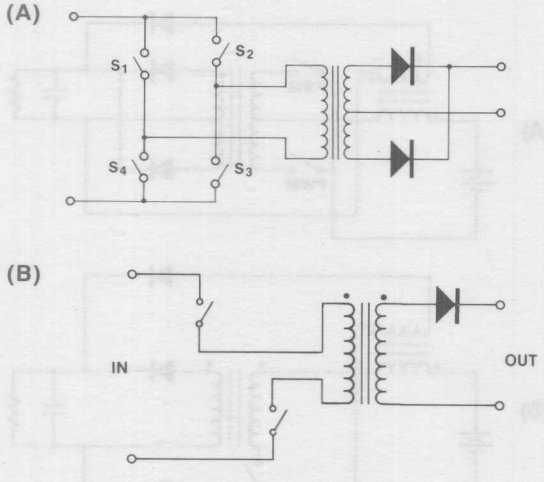


Figure 42

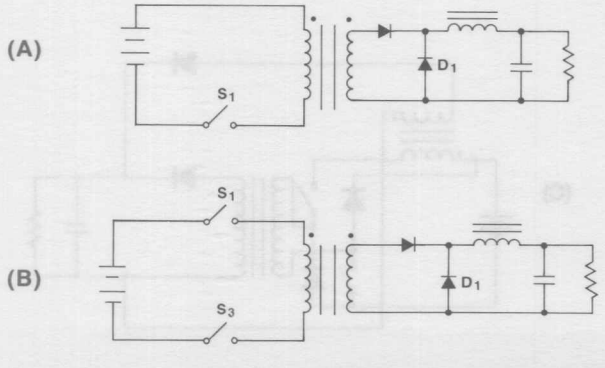


Figure 43

The designer has two choices (Figure 44); he may select a core which has a low Br and which will self discharge or he may select a very square core with little energy storage and then reset the core externally.

In the case of self-resetting, the energy may be dissipated in the primary or secondary (Figure 45), or recovered in the primary or secondary, as shown in Figures 46 and 47.

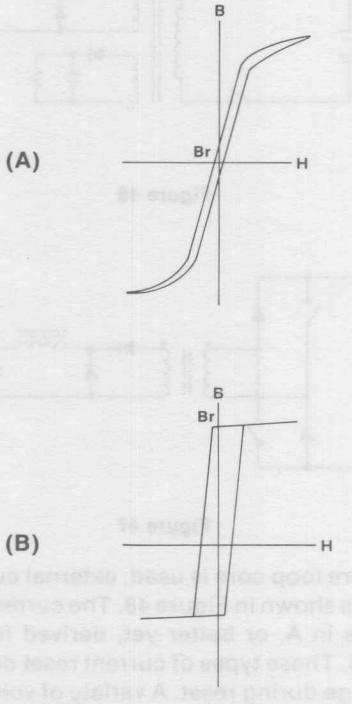


Figure 44

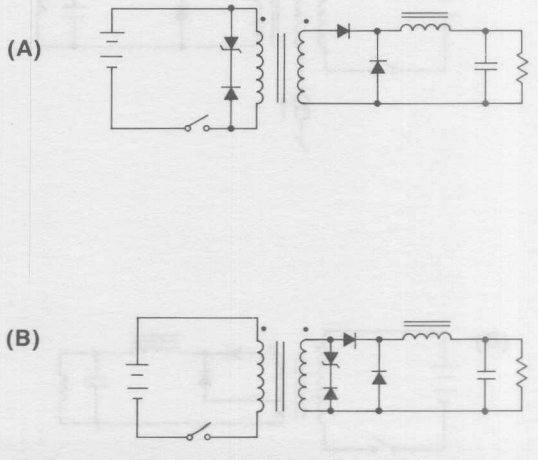


Figure 45

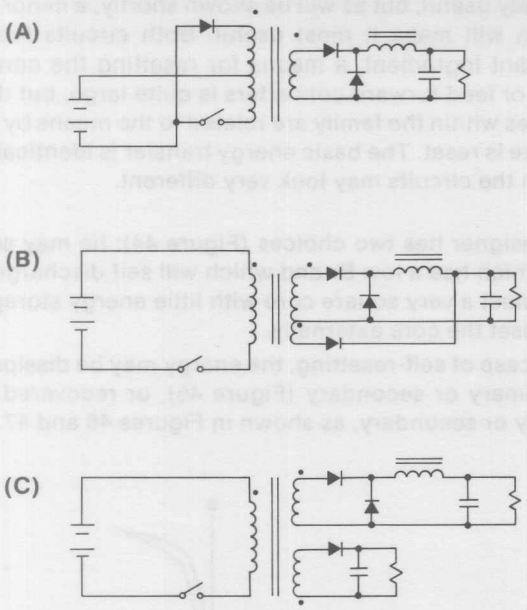


Figure 46

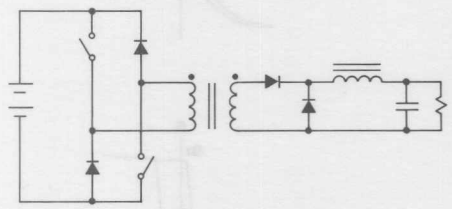


Figure 47

Where a square loop core is used, external current reset can be provided as shown in Figure 48. The current supplied by a DC source as in A, or better yet, derived from the output choke, as in B. These types of current reset do not define the winding voltage during reset. A variety of voltage clamps for current reset can be used as shown in Figure 49.

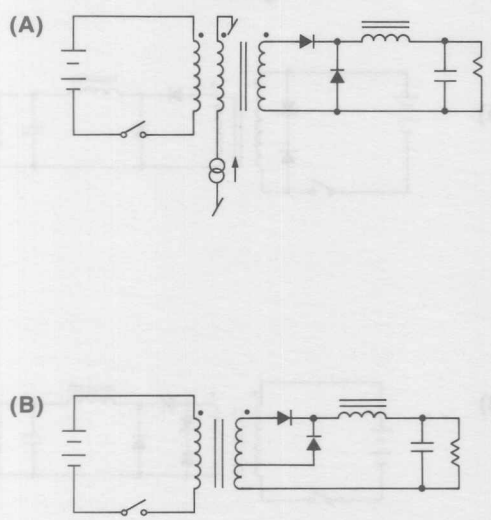


Figure 48

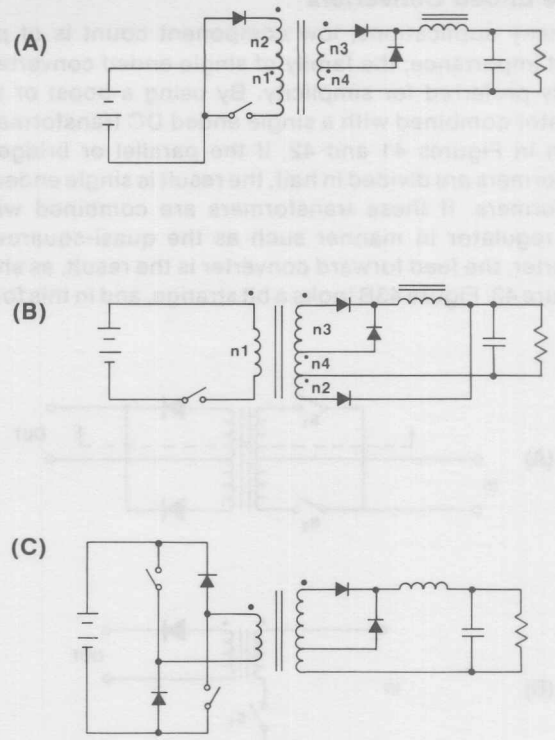


Figure 49

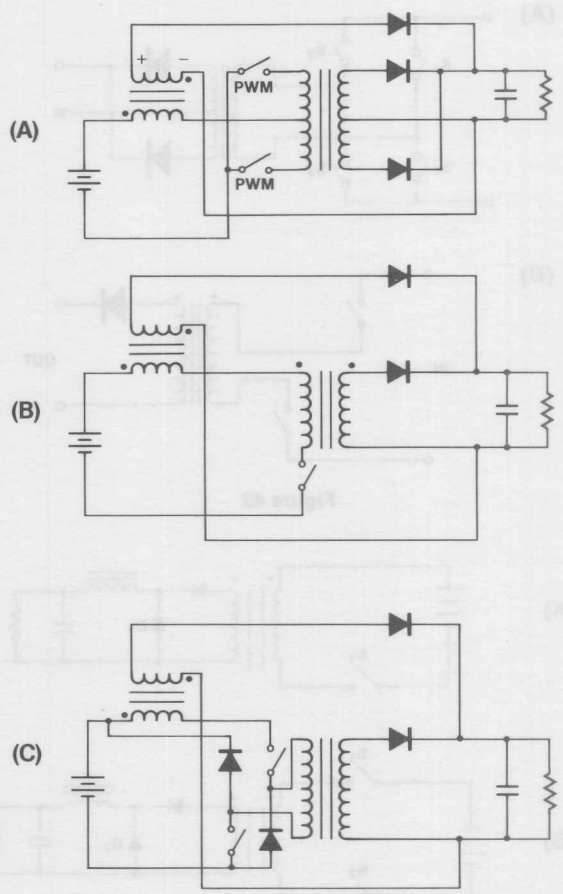


Figure 50

The quasi-squarewave converter is not the only member of the symmetrical converter family that has a single ended equivalent. As shown in Figure 50B, the Weinberg circuit (Figure 29C) is another which can be single ended. Again, the core reset means is omitted, and the designer is free to select the reset scheme and core of his choice. Figure 50C is one possible example.

Single ended versions of symmetrical boost converters can also be derived, as shown in Figure 51 where A is converted to B. To maintain current continuity in the choke, the duty cycle of S1 is now the complement of S3.

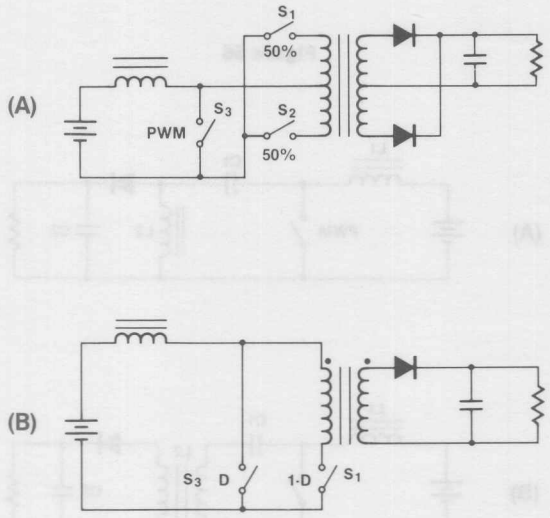


Figure 51

Limitations On This Procedure

It has been demonstrated that inserting a DC transformer into a buck or boost converter can produce a wide variety of useful topologies. The procedure does not, however, work for all regulators and all DC transformers.

For example, if a parallel connected DC transformer is inserted into a Ćuk converter, most of the combinations will not work. This is because the Ćuk converter requires a bidirectional flow of current to function, and the usual switch in the primary, rectifier in secondary DC transformer connection does not permit this. The designer must be on the lookout for this problem. For some circuits the single ended DC transformer does not provide for continuous current flow in the inductor, so that such variations don't work.

Even with these restrictions a huge number of circuits can still be developed.

SYNTHESIS USING COMBINATIONS OF CONVERTERS

A very powerful technique for deriving new circuits is to treat buck and boost regulators and the DC transformers as two port networks, and then combine these networks in various arrangements.

A few of the many possibilities are shown in Figure 52. Beginning with A, similar or dissimilar converters can be cascaded. An outstanding example of this process is the Ćuk converter (Figure 53A) which was initially derived by cascading a boost followed by a buck regulator. This topology has several important variations, as shown in Figure 53B, C and D.

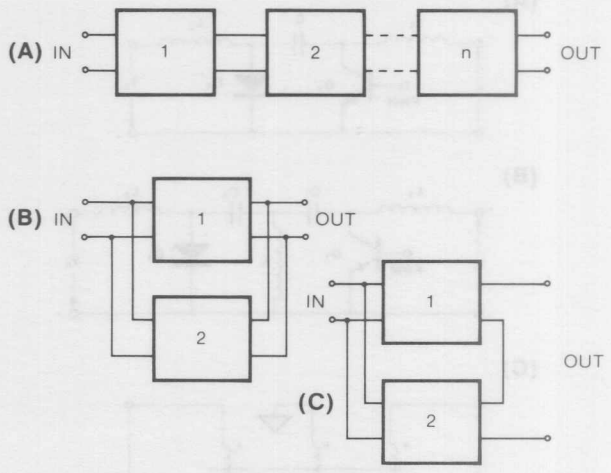


Figure 52

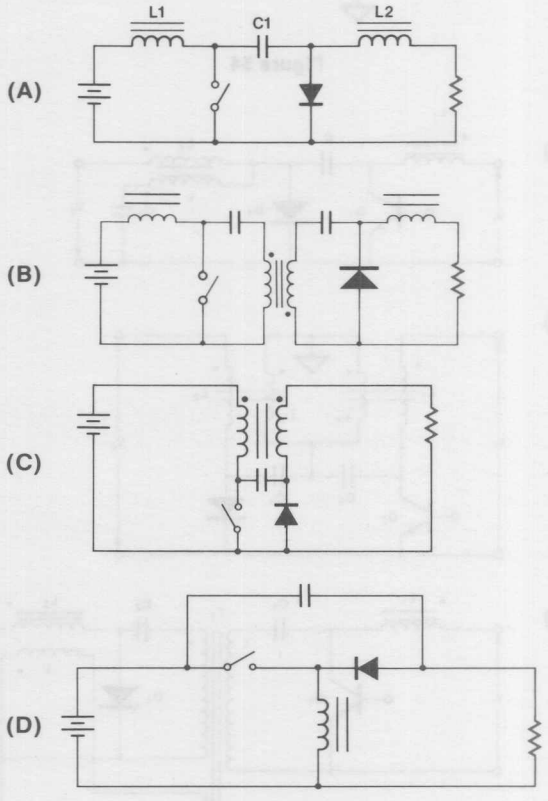


Figure 53

The Ćuk converter has the unusual property of zero input or output ripple in the coupled inductor case. By an additional circuit permutation, it is possible to have zero current ripple on *both* the input and the output. Figure 54 shows one way to accomplish this. A is the basic circuit. In B, C is divided and an inductance L is added. In C, the three inductors are coupled. Zero input and output ripple is achieved by adjusting the mutual coupling between the windings or by using trimming inductors.[37] Figure 55 shows some other variations to achieve the same goal.

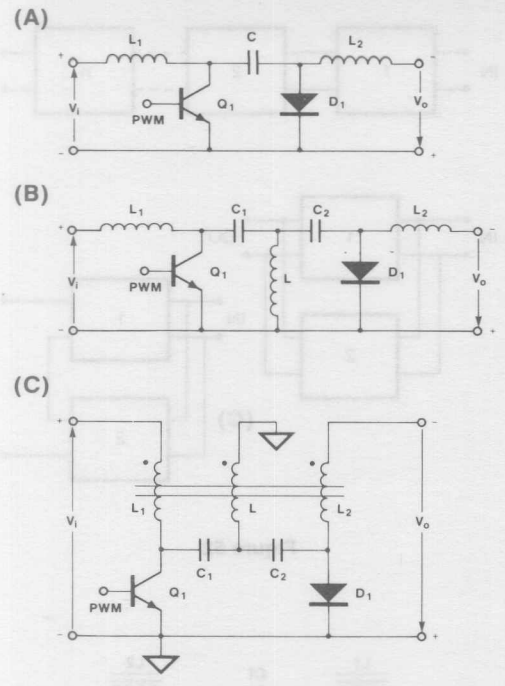


Figure 54

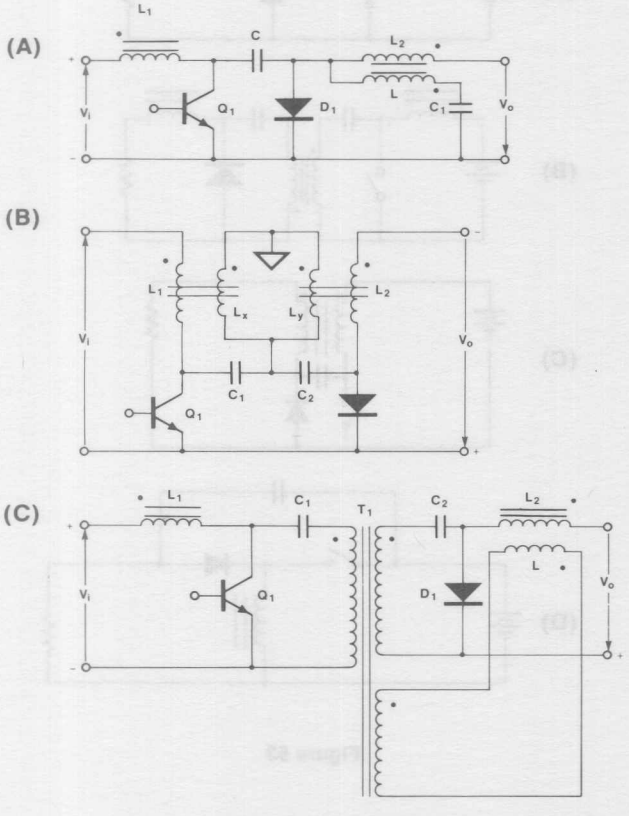


Figure 55

It can be shown that the common buck-boost regulator (Figure 56A) circuit may be derived from a cascaded connection of a buck followed by a boost regulator. By the simple expedient of using a multiple winding choke, the popular flyback converter is derived.

A cascade connection of a boost and a buck-boost is shown in Figure 57A. This can be transformer isolated in the same way as the flyback, by making L2 a multiple winding choke

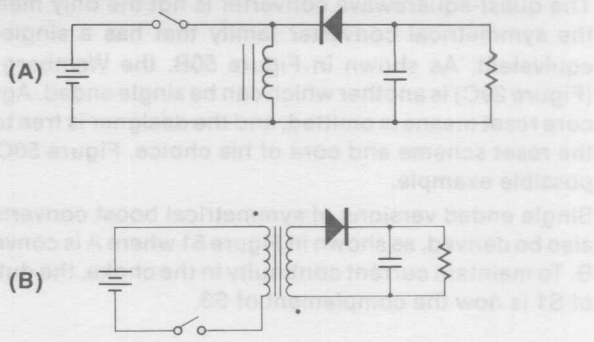


Figure 56

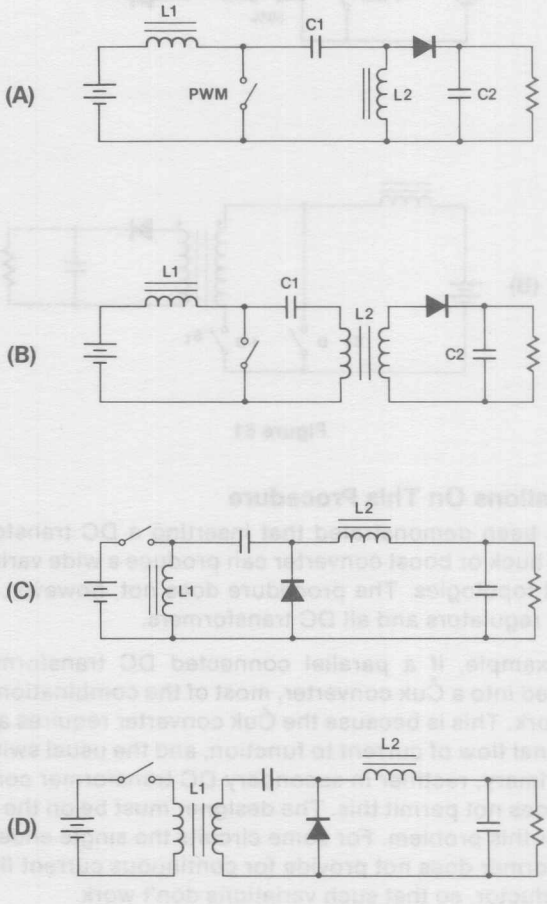


Figure 57

(Figure 57B). If duality is applied to these two circuits, the arrangements in Figure 57C and D are obtained.

Identical converters can also be cascaded with useful results. An example of this is given in Figure 58. The input to output voltage transfer ratio is:

$$\frac{V_i}{V_o} = (D)^n$$

This circuit connection can be very useful when large transformation ratios are desired. Using a single buck stage for a large transformation ratio results in very narrow, high amplitude current pulses which restrict the power handling capability of the switching device. This is a very real limitation in off-line converters. By cascading two or more converters, a

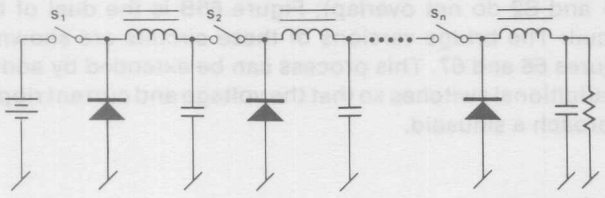


Figure 58

larger duty cycle is used which reduces the current amplitude. For example, a converter using a single stage operating with a duty cycle of 0.1 would have a duty cycle of 0.32 if changed to two stages, a three to one reduction in peak current! A second benefit is that S2 would see only 32% of the input line voltage, and could be a less expensive device than S1.

Paralleling of converters (Figure 52B) is another very useful way of increasing the power capability. By altering the switch drive phasing between the converters, the output ripple frequency can be increased and the amplitude decreased.

Cascading and paralleling are not the only possibilities. An example (Figure 52C) of connecting the inputs of two converters in parallel with their outputs in series is shown in Figure 59A. This is a combination of a DC-DC converter and a flyback converter. If bilateral inversion is applied to A, then the circuit in B results; another way to derive the circuit in Figure 29C.

The possible combinations are endless and really limited only by the designer's imagination and persistance.

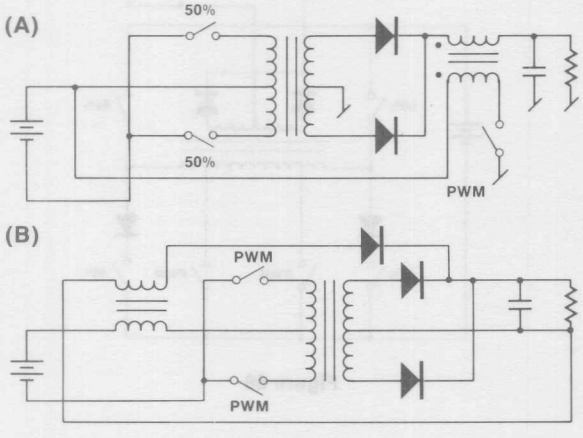


Figure 59

Limitations to the Procedure

Not all of the possible four terminal combinations yield working circuits, and general rules as to what will or will not work have not yet been derived. The designer must, for the present, use a cut and try approach.

SYNTHESIS USING TRANSFORMER AND INDUCTOR TAPPING

A very simple way to modify known circuits in useful ways employs tapping of the inductor and/or transformer.

Inductor Tapping

One of the simplest modifications is to tap the inductor to alter the component voltage or current stress, as shown in Figure 60.

The concept of tapping the inductor may be extended to the use of multiple windings. It has been shown that the multiple wound inductor can be used in place of multiple inductors, as shown in Figure 61, with a significant savings in size and weight.

A circuit using a two winding choke can also be used to reduce the size of a filter capacitor as shown in Figure 62.

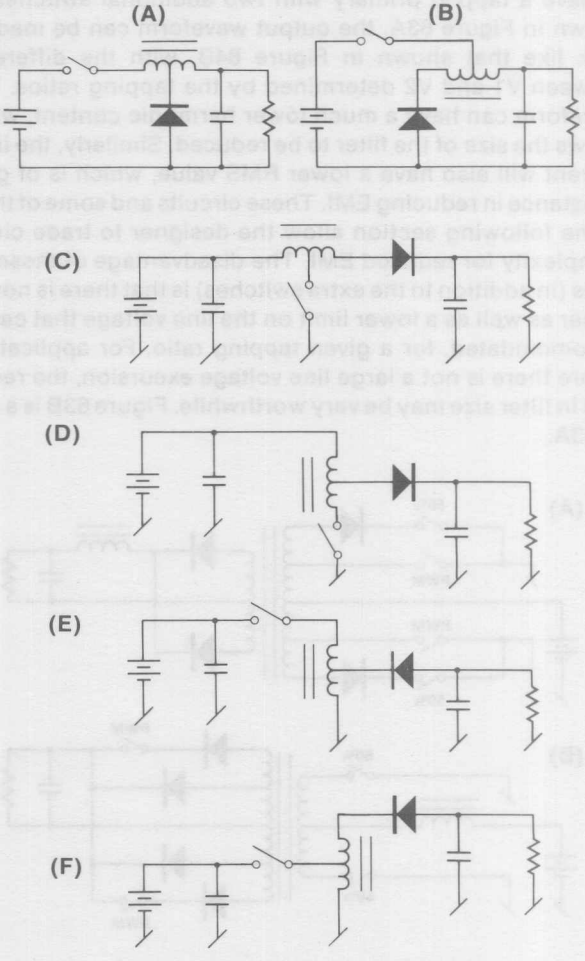


Figure 60

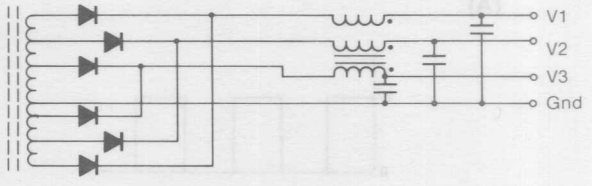


Figure 61

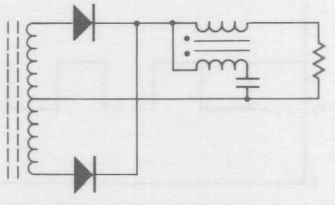


Figure 62

Transformer Tapping

The transformer may be tapped to provide very useful circuit variations. Figures 63 and 65 show some examples. The quasi-squarewave circuit has an output voltage waveform (before the filter) like that shown in Figure 64A. This waveform has a very high harmonic content which must be dealt with by the filter. If the quasi-squarewave circuit is modified to have a tapped primary with two additional switches, as shown in Figure 63A, the output waveform can be made to look like that shown in Figure 64B, with the difference between V1 and V2 determined by the tapping ratios. This waveform can have a much lower harmonic content, which allows the size of the filter to be reduced. Similarly, the input current will also have a lower RMS value, which is of great assistance in reducing EMI. These circuits and some of those in the following section allow the designer to trade circuit complexity for reduced EMI. The disadvantage of these circuits (in addition to the extra switches) is that there is now an upper as well as a lower limit on the line voltage that can be accommodated, for a given tapping ratio. For applications where there is not a large line voltage excursion, the reduction in filter size may be very worthwhile. Figure 63B is a dual of 63A.

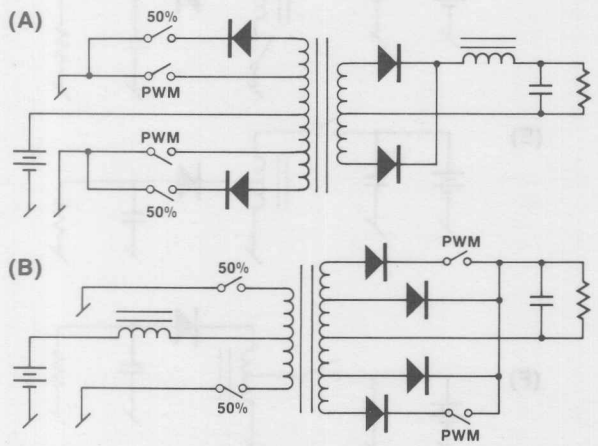


Figure 63

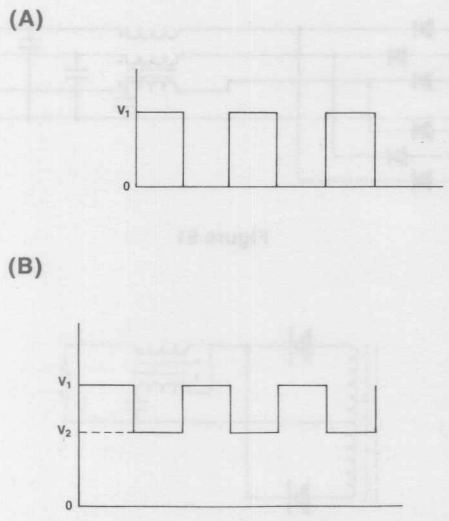


Figure 64: Converter Output Voltage Waveform

Figure 65A is a boost derived circuit using the same principle (S1 and S2 do not overlap); Figure 65B is the dual of this circuit. The bridge versions of these circuits are shown in Figures 66 and 67. This process can be extended by adding 2n additional switches so that the voltage and current ripples approach a sinusoid.

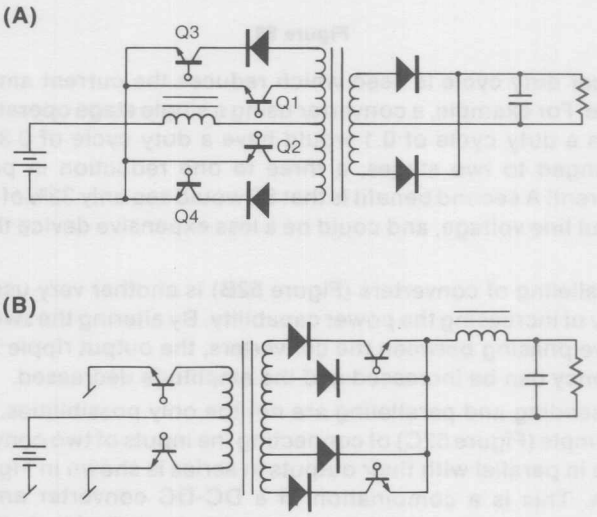


Figure 65

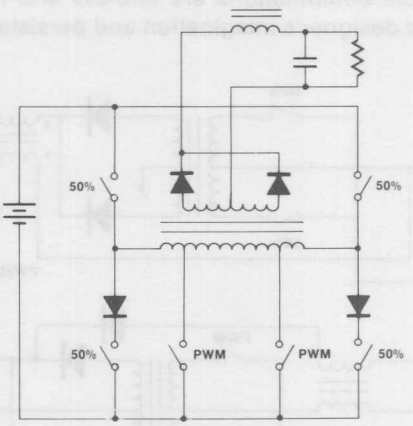


Figure 66

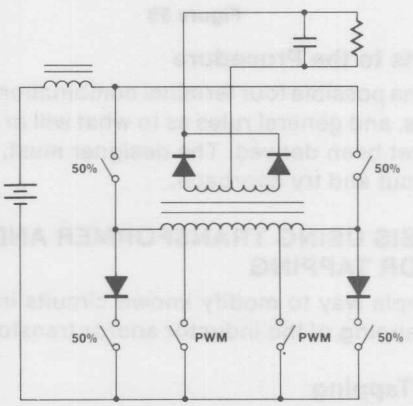


Figure 67

Combined Choke and Transformer Tapping

Tapping of both the choke and the transformer can be combined in one converter. An example of this is shown in Figure 68A, along with its dual, 68B. By tapping the choke, the output current becomes continuous and the input discontinuous. Figure 69 shows the bridge version of Figure 68A.

By tapping the inductor and transformer in the circuit in Figure 70A, the circuit in 70B is generated. This circuit has the advantage of reducing the current in D1 and D2, increasing the circuit efficiency while retaining the continuous output current and current-fed converter nature. This particular combination of tapping does not have the upper limit on input voltage.

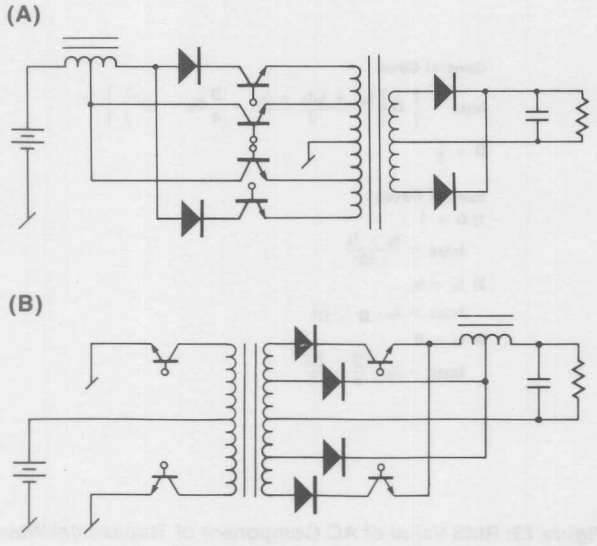


Figure 68

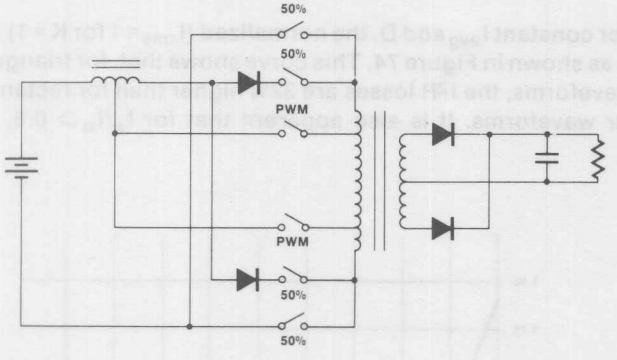


Figure 69

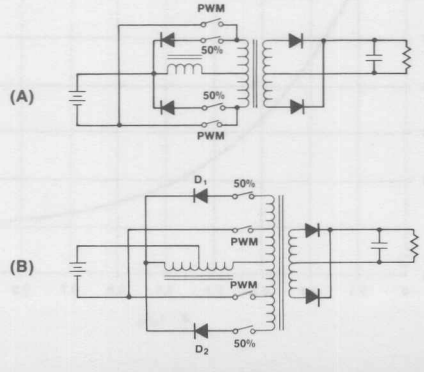


Figure 70

SUMMARY

A wide range of ideas and techniques, many of which are new, have been presented herein. So much has been presented that the reader may find it difficult to see the forest as opposed to the individual trees.

The key ideas that have been presented are:

1. The present popular circuits represent only a small portion of switchmode converter possibilities. The popular circuits are not the only, or even the best, solutions.
2. The designer is not restricted to using the present known converter circuits but can, by modifying the known circuits and synthesizing new ones, derive new circuits to better solve his problem.
3. All of the converter topologies we presently know can be derived from combinations of very simple elements; the buck and boost regulators and some form of DC transformer.
4. Converter topologies can be grouped into families with similar characteristics. One way to perform this grouping is to define the family members on the basis of the basic circuit elements from which the individual circuits are derived.
5. General duality theory can be applied to switchmode converters to provide both insight into circuit relationships and a synthesis tool.
6. A special case of duality, bilateral inversion, leads directly to the use of overlapping and non-overlapping conduction and combinations thereof to alter circuit operation.
7. Bilateral inversion also leads to using rectifier connections as switch connections. This can be extended to multiplier and possibly multiphase connections.
8. Quantitative figures of merit based on component stress and energy storage, and qualitative circuit considerations can be used to compare circuits. Comparisons of large numbers of circuits, in fact, require the use of some orderly process.
9. There are several techniques for modifying known circuits or generating new circuits: duality, bilateral inversion, combinations of boost or buck regulators with DC transformers, combinations of more complex converters, transformer and inductor tapping and, of course, combinations of all these techniques.
10. The designer is free to choose many of the circuit properties, for example: the regulation function may be performed in either the primary, the secondary or in an isolated winding. The control loop transfer function can be altered to either add or remove moving poles and right half-plane zeros. The high current ripple can be moved from the primary to the secondary or vice versa. Both primary and secondary ripple can be reduced at the expense of input voltage range or circuit complexity. By altering the switch conduction modes, the input voltage range can be greatly extended.

APPENDIX I

Effect of Waveform on RMS Value

In a switch mode converter, the current waveforms through the inductors, transformer windings, rectifiers and switches will appear, as shown in Figure 72, ranging from a triangle to a rectangle depending on the value of the averaging inductor and the load. For the capacitors, the waveforms will be similar, except that there can be no DC component, as shown in Figure 73. The RMS and average values of the waveform are given in the figures.

It can be shown that:

$$K \equiv \frac{I_a}{I_b} = f(L/L_c) \qquad (1)$$

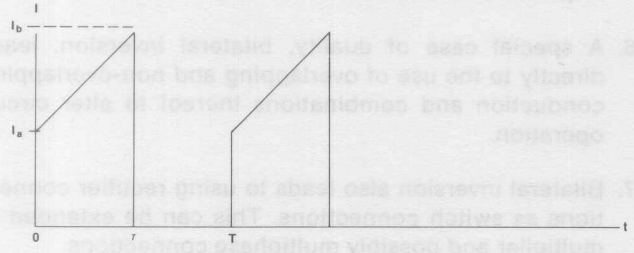
where, L = inductance of the averaging choke

L_c = is the critical inductance for a particular input voltage and load power.

As L is increased, K goes from 0 (triangle) to 1 (rectangle).

Substituting $K = I_a/I_b$, for the continuous choke current case:

$$I_{rms} = \frac{2\, I_{avg}}{\sqrt{D}} \sqrt{\frac{K^2 + K + 1}{3\,(K+1)^2}} \qquad (2)$$



General Case

$I_{AVG} = D\left(\frac{I_a + I_b}{2}\right)$

$I_{RMS} = \left[\frac{D}{3}\left(I_a^2 + I_aI_b + I_b^2\right)\right]^{1/2}$

$D = \frac{\tau}{T}$

Special Cases

1) D = 1

$I_{AVG} = \frac{I_a + I_b}{2}$

$I_{RMS} = \left(\frac{I_a^2 + I_aI_b + I_b^2}{3}\right)^{1/2}$

2) $I_a = I_b$

$I_{AVG} = I_aD$

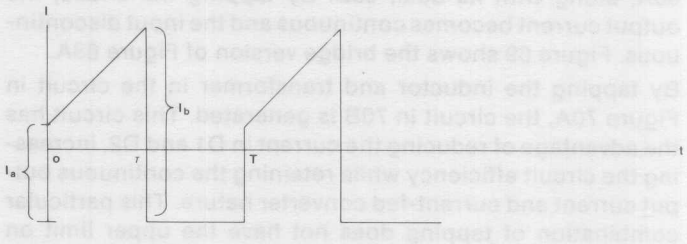
$I_{RMS} = I_a\sqrt{D}$

3) $I_a = 0$

$I_{AVG} = \frac{I_bD}{2}$

$I_{RMS} = I_b\sqrt{\frac{D}{3}}$

Figure 72: Average and RMS Values for Trapazoidal Waveform



General Case

$I_{RMS} = \left\{ D\left[\frac{I_a^2 + I_aI_b + I_b^2}{3} - \frac{D}{4}(I_a + I_b)^2\right]\right\}^{1/2}$

$D = \frac{\tau}{T}$

Special Cases

1) D = 1

$I_{RMS} = \frac{I_b - I_a}{\sqrt{12}}$

2) $I_a = I_b$

$I_{RMS} = I_a\sqrt{D - D^2}$

3) $I_a = 0$

$I_{RMS} = I_b\sqrt{\frac{D}{3} - \frac{D^2}{4}}$

Figure 73: RMS Value of AC Component of Trapazoidal Waveform

For constant I_{avg} and D, the normalized ($I_{rms} = 1$ for K = 1) I_{rms} is as shown in Figure 74. This curve shows that, for triangular waveforms, the I^2R losses are 32% higher than for rectangular waveforms. It is also apparent that for $I_a/I_b > 0.6$, the

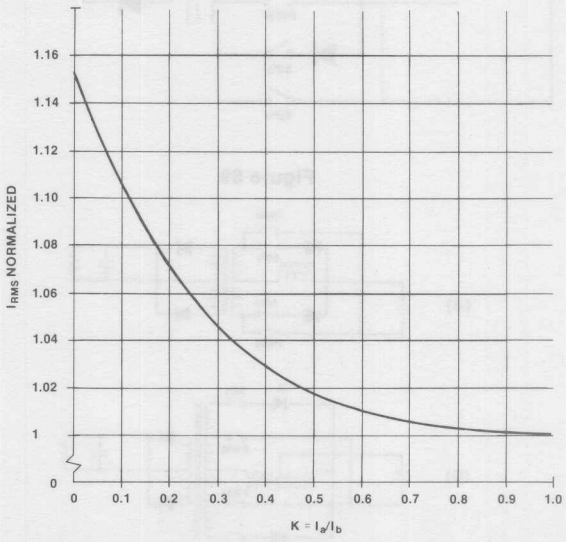


Figure 74

additional losses incurred by having $L < \propto$ is only 2%, so from a practical point of view L need only be about twice L_c. Increasing the value of I_a/I_b increases the switch turn-on losses but decreases the turn-off losses. Since the turn-off losses usually dominate, increasing I_a/I_b reduces the total switch loss also.

For the case of discontinuous inductor current ($L < L_c$), $I_a/I_b = 0$ and is no longer relevant, since the waveforms are now triangles. For a given I_{avg} the RMS current is:

$$I_{rms} = \frac{2\, I_{avg}}{\sqrt{3D}} \qquad (3)$$

A plot of equation (3) is given in Figure 75, where I_{avg} is constant and I_{rms} is normalized for D = 1. Obviously triangular current waveforms with high peak currents and low duty cycles are to be avoided if low losses are desired.

For the case where: $I_a = I_b$:

$$I_{rms} = \frac{I_{avg}}{D}$$

the curve in Figure 75 also applies. It is important to realize that for a given input voltage, current and transformation ratio, there can be a difference in duty cycle which allows one circuit to have lower losses due to the lower value of I_{rms}.

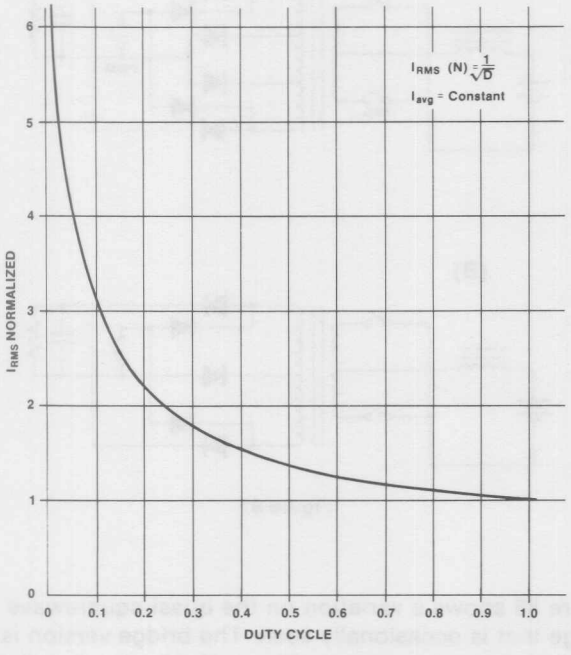


Figure 75: Variation of RMS Current with Duty Cycle.

APPENDIX II

Despite the huge number of circuits presented in the main portion of this application note, there are still many more that could be shown. To provide the reader with as full a picture as possible, some additional circuits are presented here with limited comment.

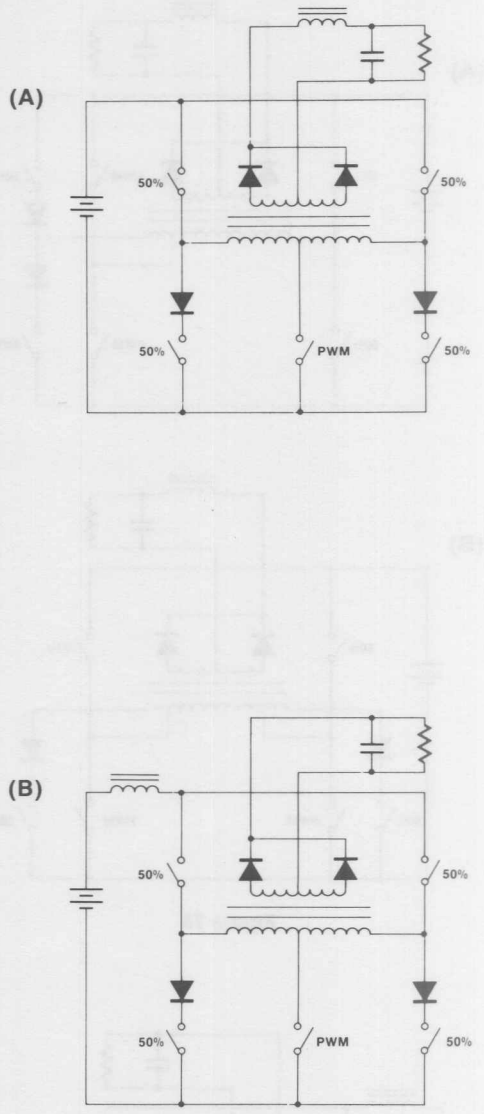


Figure 76

The circuits shown in Figures 63 through 69 have a number of additional variations. When the input voltage range is 2:1 or less, one switch may be eliminated as shown in Figures 76 and 77; the switch connections can also be varied as shown in

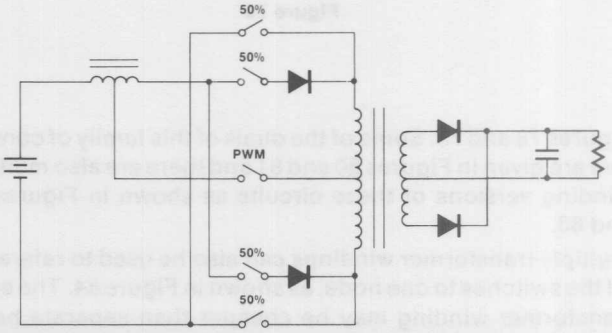


Figure 77

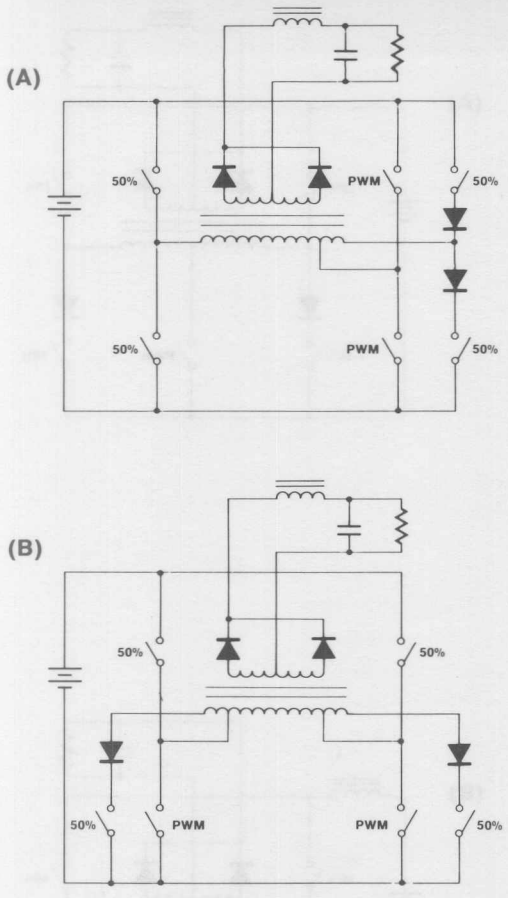


Figure 78

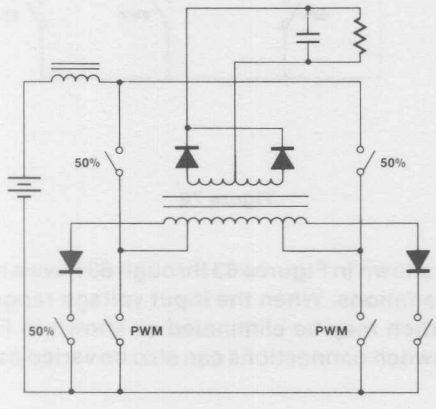


Figure 79

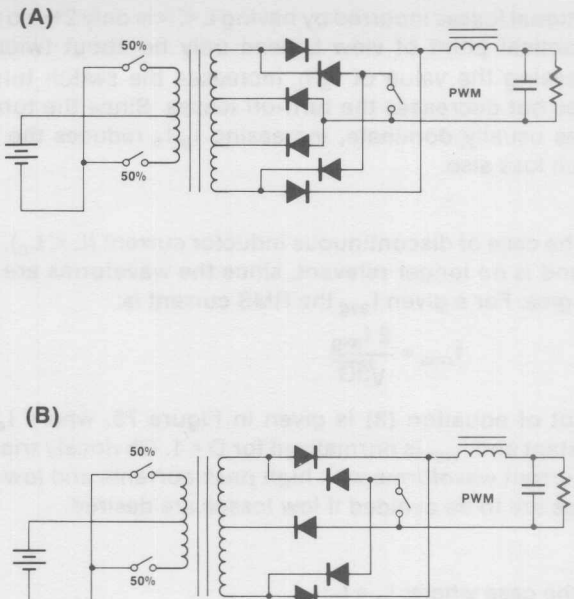


Figure 80

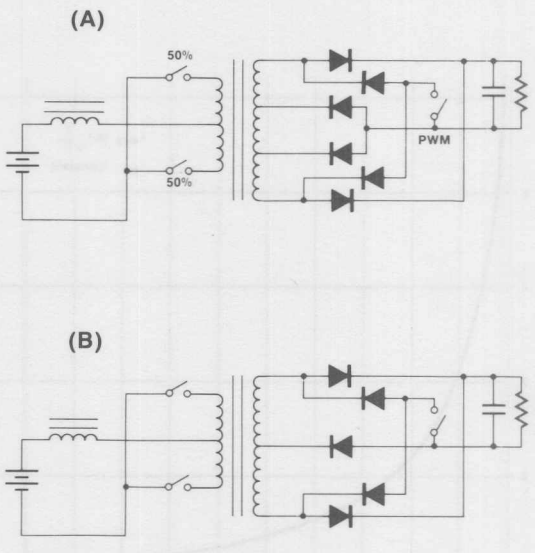


Figure 81

Figures 78 and 79. Some of the duals of this family of converters are given in Figures 80 and 81 and there are also multiple winding versions of these circuits as shown in Figures 82 and 83.

Multiple transformer windings can also be used to reference all the switches to one node, as shown in Figure 84. The extra transformer winding may be cheaper than separate base/gate drive isolation transformers, however, there will be some voltage spiking due to leakage inductances between the primary windings.

Figure 85 shows a variation on the quasi-squarewave half-bridge that is occasionally seen. The bridge version is also possible. The major disadvantage of this circuit is that the inductor must operate in the discontinuous mode. Two more useful variations of this circuit are shown in Figure 86. In A, S1 and S2 use overlapping or nonoverlapping conduction, and in B, the PWM switch is in the secondary. Bridge versions of both these circuits can be built, with and without dual chokes.

The circuit in Figure 87 is a variation of that previously given in Figure 51B. In this variation, T1 is designed to store energy while L1 is discharging through the transformer into the load (S1 open, S2 closed). While energy is being stored in L1 (S1 closed, S2 open), the transformer discharges into the load. If

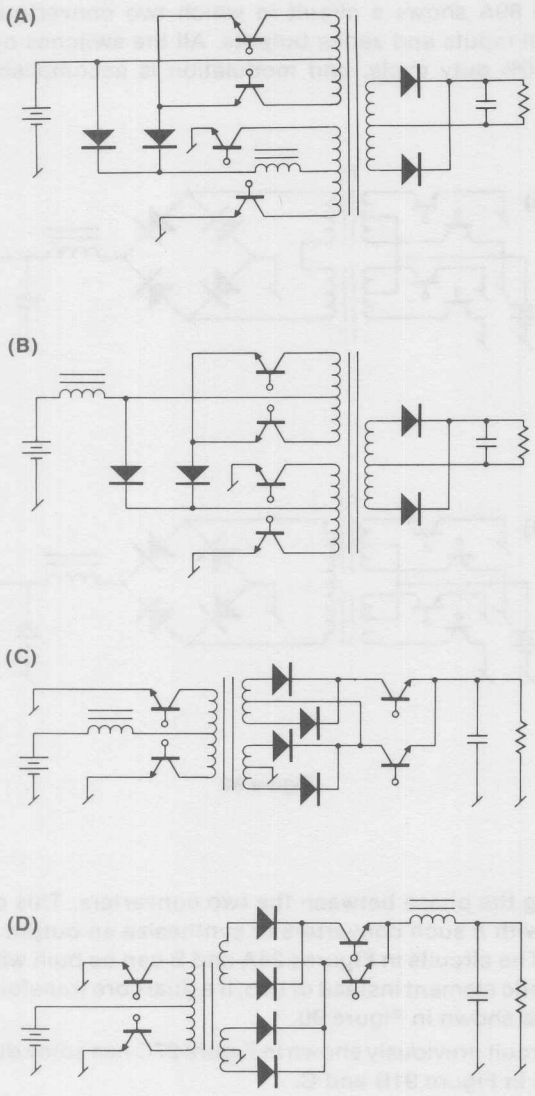


Figure 82

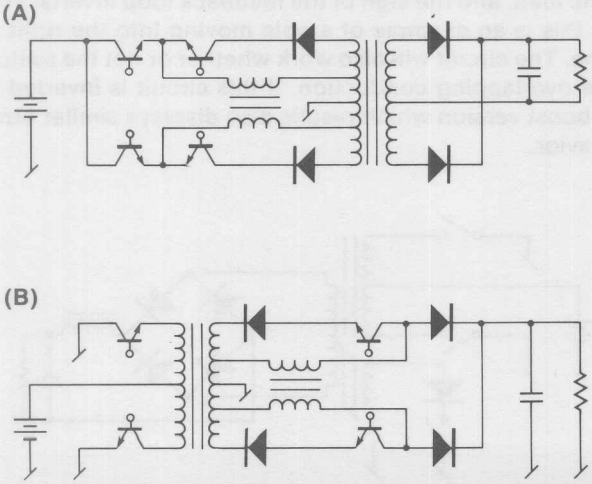


Figure 83

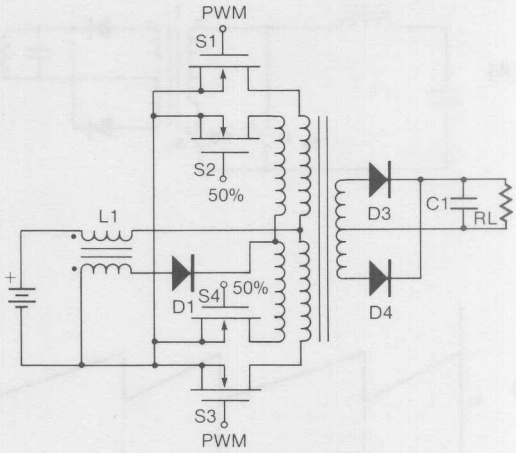


Figure 84

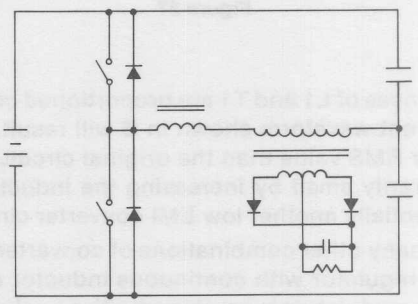


Figure 85

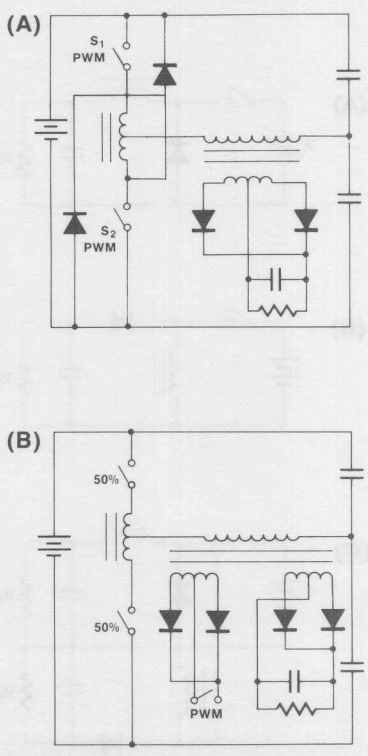


Figure 86

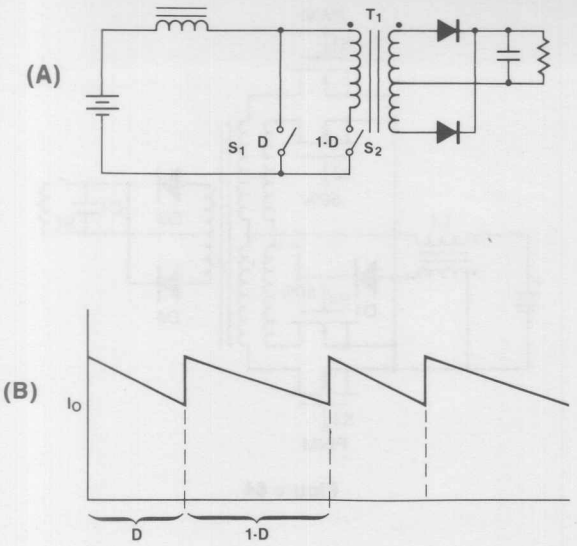


Figure 87

the inductances of L1 and T1 are proportioned correctly, the output current waveform shown in B will result. This has a much lower RMS value than the original circuit and can be made arbitrarily small by increasing the inductance value. This is potentially another low EMI converter circuit.

There are many other combinations of converters. In Figure 88, a buck regulator with continuous inductor current and pulse width modulation is combined with a buck-boost regulator having discontinuous inductor current and variable frequency. The two are combined with PWM and variable frequency control loops to produce a converter with a single switch and two independently regulated outputs.

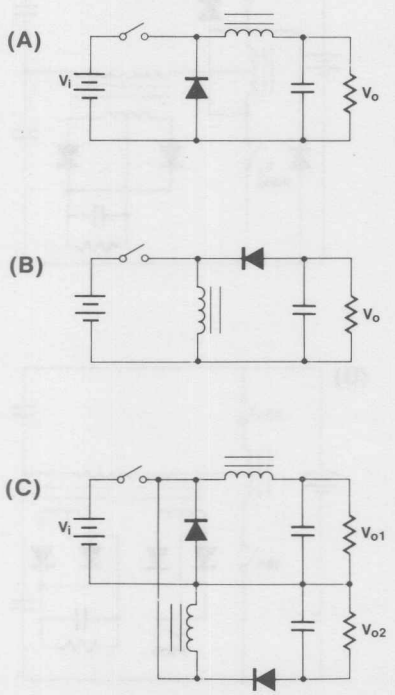


Figure 88

Figure 89A shows a circuit in which two converters have parallel inputs and series outputs. All the switches operate with 50% duty cycle, and modulation is accomplished by

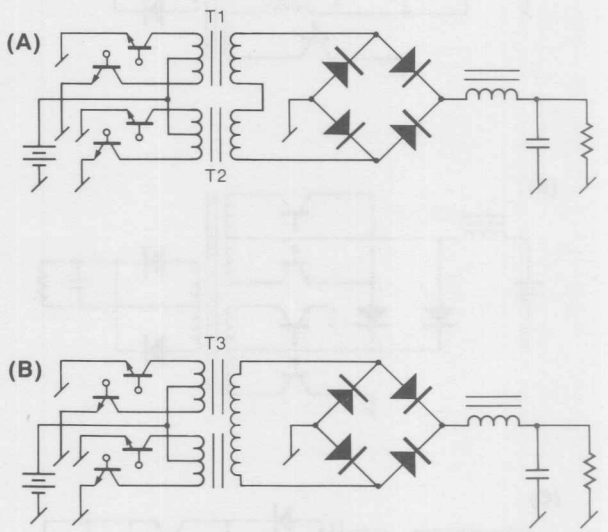


Figure 89

varying the phase between the two converters. This can be done with *n* such converters to synthesize an output waveform. The circuits in Figures 24A and B can be built with one magnetic element instead of two, if a dual core transformer is used as shown in Figure 90.

The circuit previously shown in Figure 27C has some duals as shown in Figure 91B and C.

The circuit in Figure 28C can be reconnected to be similar to that of Figure 26D as shown in Figure 92.

A variation using a tapped choke is shown in Figure 93A. This circuit is interesting in that some of the energy stored in the inductor is returned to the source rather than to the load. The circuit has the unusual property that at certain duty cycles more power is pumped back into the source than is delivered to the load, and the sign of the feedback loop inverts! Possibly, this is an example of a pole moving into the right half plane. The circuit will also work whether or not the switches have overlapping conduction. If this circuit is inverted (B), the boost version which results also displays similar bizarre behavior.

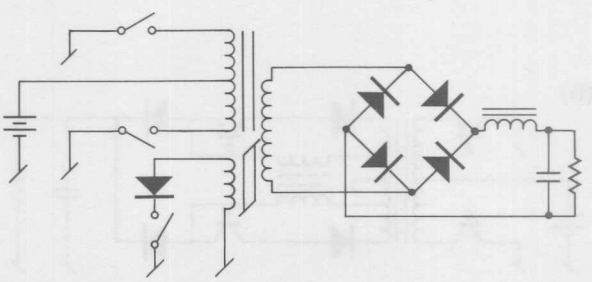


Figure 90

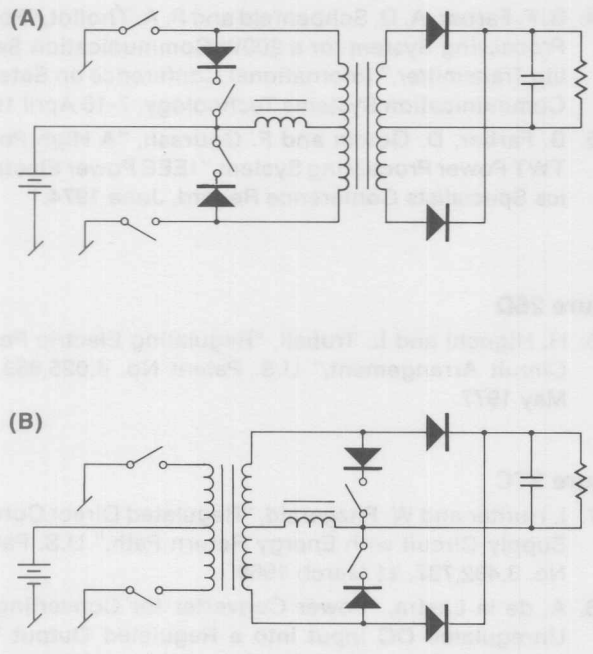


Figure 91

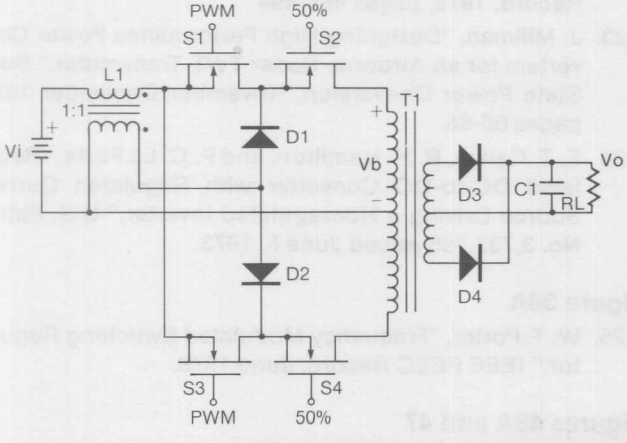


Figure 92

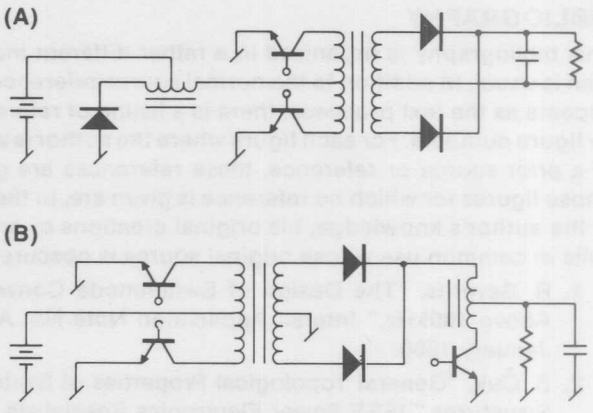


Figure 93

A few of the circuits previously shown (Figures 30C, 46A, 47, 49A, 50, 86 and 94) also return energy to the source, and it is conceivable that all these circuits can display this type of instability. In some cases, this can be prevented by limiting the stored energy, but not always.

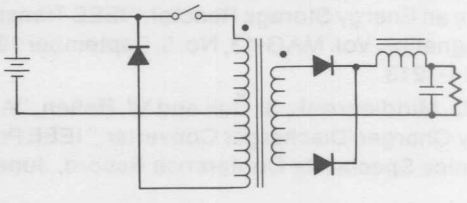
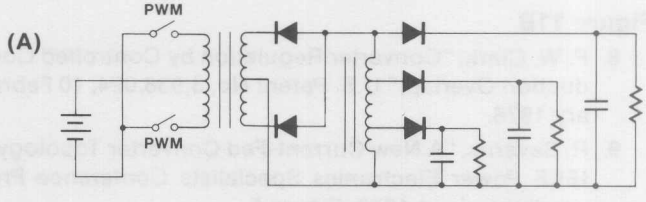


Figure 94



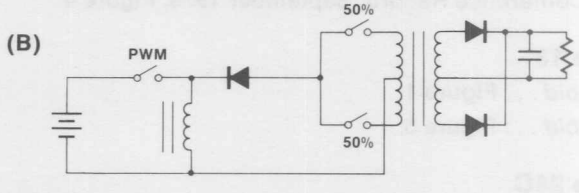


Figure 95

ACKNOWLEDGEMENT

The author would like to express his appreciation to Dr. Slobodan Ćuk for allowing the reprinting of a portion of his PESC '79 paper and to Ed Bloom of Litton Guidance and Control and Trey Burns of Digital Equipment Corporation for reviewing and commenting on the manuscript.

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This bibliography is organized in a rather different manner than is usual. In addition to the normal source reference that appears as the text proceeds, there is a listing of references by figure numbers. For each figure where the author is aware of a prior source or reference, these references are given. Those figures for which no reference is given are, to the best of the author's knowledge, his original creations or are circuits in common use whose original source is obscure.

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Figure 13

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INTERSIL

10710 N. Tantau Avenue, Cupertino, CA 95014 U.S.A., Tel: (408) 996-5000, TWX: 910-338-0171
9th Floor, Snamprogetti House, Basing View, Basingstoke, RG21 2YS, Hampshire, England, Tel: 0256-57361, TLX: 847227 INTRSL G
217, Bureaux de la Colline, de St. Cloud, Batiment D, 92213 Saint-Cloud, Cedex, France, Tel: (1) 602-57-11, TLX: Datelem 204280F
Bavariaring 8, 8000 Munchen 2, West Germany, Tel: 89/539271, TLX: 5215736 INSL D